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AUTOMATIC TEST METHODS FOR LINEAR MICROCIRCUITS.(U)
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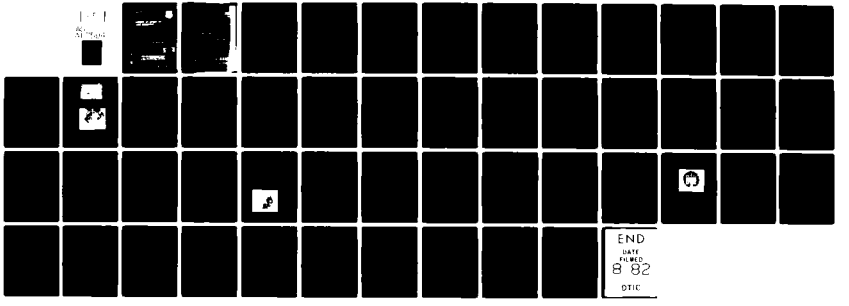

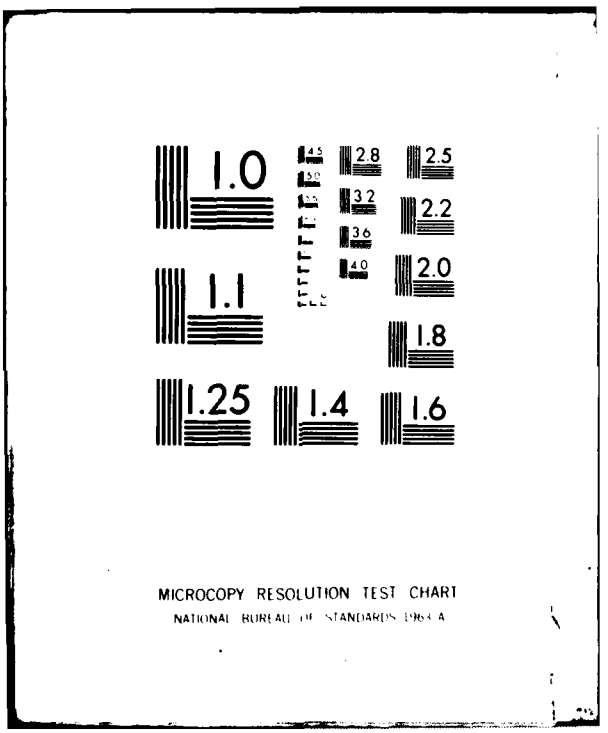
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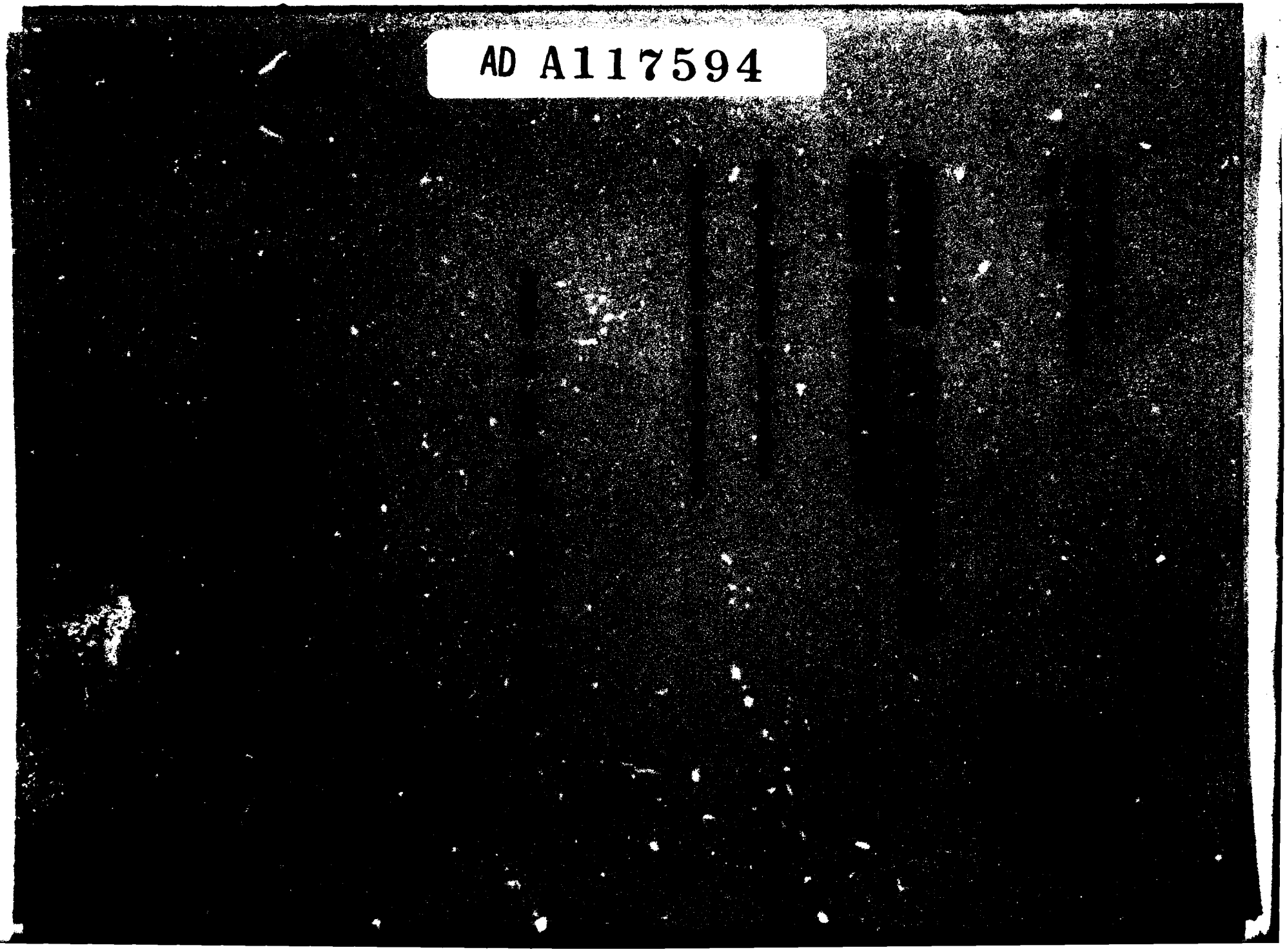
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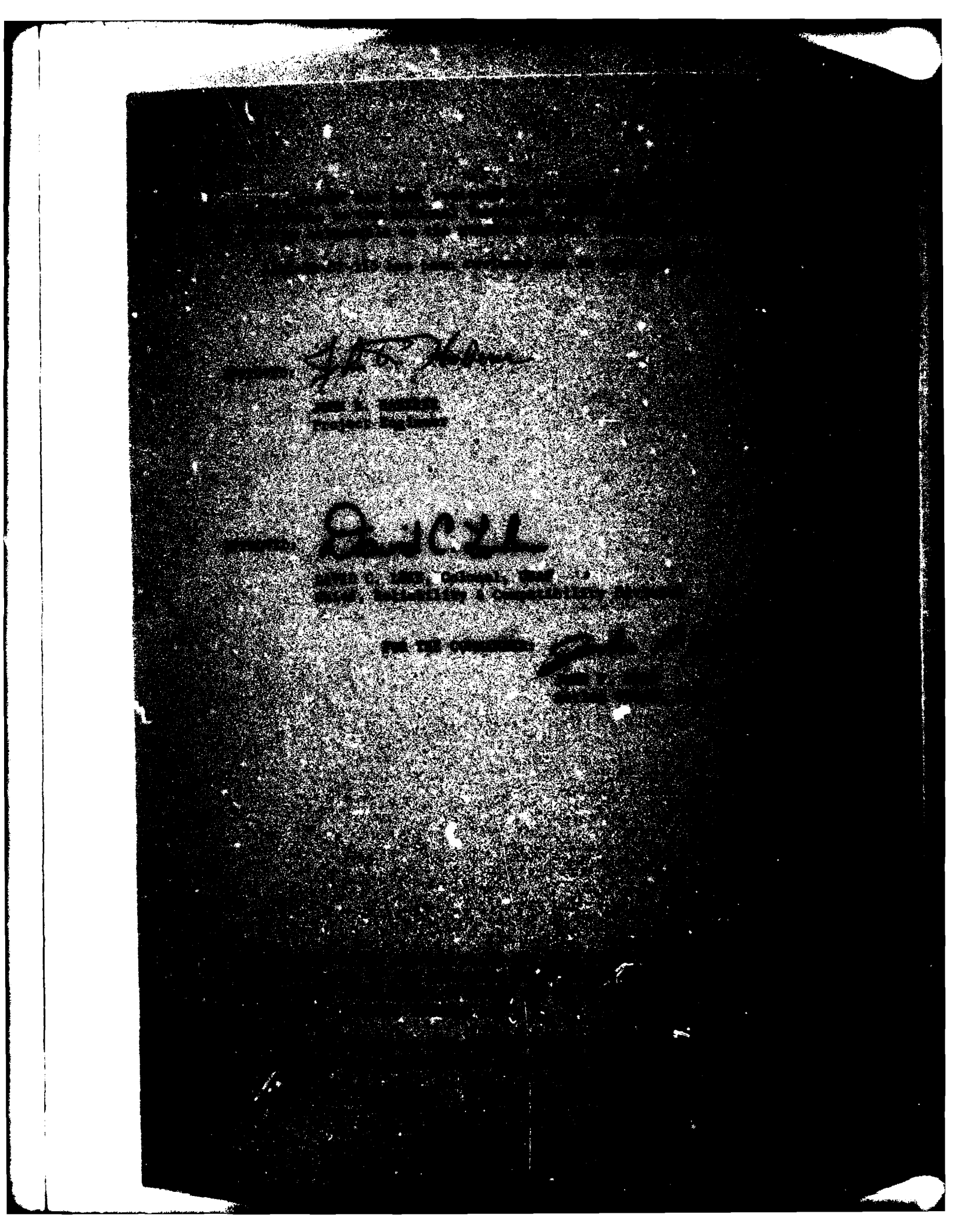

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MIL-M-38510 slash sheets	Gain measurements

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The objective of this effort was to review MIL-M-38510 operational amplifier and comparator electrical test conditions, and to develop simplified test procedures of these parts on general purpose automatic test equipment. There was an emphasis on gain measurements. However, all parameters were investigated for implementation on ATE as well as the effects of accuracy, repeatability, and chip heating. Modifications to MIL-M-38510 slash sheets are recommended, as well as additions to same.

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EVALUATION.

This effort addressed the testing of specific linear device types using general purpose digital automated test equipment (ATE). The device types used as test vehicles included the M-38510/10104, 10107, 11901 (LM108A, LM118, TL061 operational amplifiers and the M-38510/10304 (LM111) comparator. Interface adaptors and test procedures were evaluated to determine the test repeatability and accuracy that could be obtained using various approaches and comparing to bench test methods. Alternative testing techniques that eliminate the null amplifier used in the MIL-M-38510 approach and take advantage of the iterative power of ATE were evaluated. Especially difficult tests such as current measurements in the picoampere range and AC measurements such as rise time, overshoot, settling time, and slew rate were evaluated to determine the best possible implementation. Most of the techniques evaluated attempt to improve accuracy and repeatability, however at the expense of a considerable increase in test time due to the requirement that test conditions be iterated to achieve a given measurement result. In some cases, the resultant increase in test time would be unacceptable if testing were being performed as a 100 percent screen.

The general observation can be made that although the techniques developed and applied in this study use somewhat fewer components, the typical accuracies obtained do not give any significant improvement over the test methods currently being specified in the relevant MIL-M-38510 slash sheets. The advantage of requiring somewhat fewer components to implement the studied techniques is offset by the requirement that accurately premeasured resistors be used during construction of the test fixture and these values included in the test program. If several test fixtures were built for a given device, it would be necessary that the test program use the measured resistance values on the test fixture actually in use

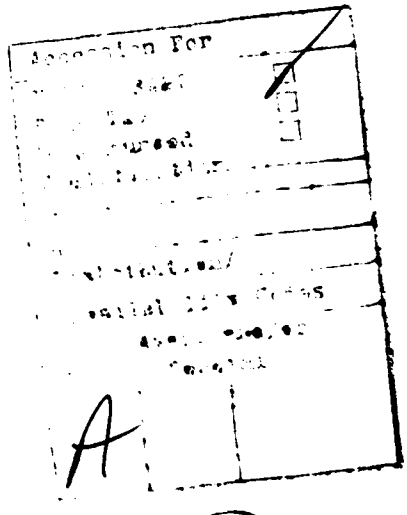
or the expected measurement accuracy would not be achieved. Another potential disadvantage of the proposed test implementation is encountered when read and record data is required. Since a null amplifier is not used to establish the desired operating point on some tests, the conditions must be varied in an incrementally iterative manner to obtain an actual value for these parameters. This can require typically 10 to 100 tries to establish each required parameter value. This increases test time by up to 100 times that required when using a null amplifier technique and could be prohibitive when testing large quantities. If however a simple go/no go indication is needed, this disadvantage is eliminated. An additional trade-off that must be considered is the increase in program complexity incurred as a result of the test fixture hardware simplification.

The test accuracies as presented in this report must be applied only to the specific measurement and related test conditions under which they were calculated. Some of the accuracies are expressed as a percent of the specification limit for a defined measurement system range and loop gain. Others are expressed as a percent of typical value. The text should be carefully read to establish the exact basis for each accuracy figure given.

All of the proposed techniques were developed and applied at room temperature and no attempt has been made to ensure that they can be used at temperature extremes. For example, the measurement of input bias current as discussed on page 12 of this report assumes a 2 nanoampere limit for the 38510/10104 (the room temperature limit). Using the technique as discussed, the maximum value that can be measured is $\pm$ 2 nanoampere before the measurement range must be changed. At -55^{o}C where the limit is $\pm$ 3 nanoampere, the measurement system range must be changed resulting in a degradation of the accuracy figure which has been given.

The test techniques as presented have established that it is feasible to test linear microcircuits on general purpose digital automated microcircuit test equipment without using the conventional null amplifier approach to stabalize the operating point of a device being tested. Some of the potential problem areas mentioned in this evaluation may be a factor, however some areas of improvement do warrant consideration. In particular past stability problems associated with testing the 38510/103 comparator appear to have been eliminated with the simplified test circuit as presented in this report. The real problem area, that of accurately measuring the transient response performance characteristics in an automated environment, was evaluated to a limited extent in this study. These measurements can be made but at a substantial increase in test fixture interface hardware. These issues should be addressed in the future with the goal of achieving complete automation of these tests (which are often bench tests at present) capable of providing accurate repeatable results on the same fixture as used for the static performance measurements.

JOHN R. HABERER
RADC Project Engineer



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Preface

This work was funded by the Rome Air Development Center (RADC) under the provisions of contract F30602-80-C-0184 to provide a basis for revisions to test methods and procedures contained in MIL-STD-883 and MIL-M-38510 slash sheets. The specific emphasis of this work was on selected linear microcircuits tested with general purpose automatic test equipment (ATE).

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ILLUSTRATIONS

TABLES

I. SUMMARY

1. TECHNICAL PROBLEM

The standards for high reliability testing of linear integrated circuits are contained in MIL-STD-883 and MIL-M-38510. The purpose of this study was to address problems involved with the use of general purpose automatic test equipment (ATE) in meeting these standards. It is important to note that all ATE references in this report refer to general purpose test equipment commonly used for digital microcircuit testing.

2. METHOLOLOGY

Test fixtures were constructed and test programs written for four preselected linear integrated circuits and used to evaluate the existing MIL-M-38510 test methods. Certain tests were performed on automatic test equipment, the fixture and test methods were then modified to achieve maximum accuracy and repeatability. The automatic test equipment used in this study were two Tektronix model S-3260 test systems, representative of general purpose automatic test equipment. An industry survey was also performed to examine the opinions of other users and suppliers of linear microcircuits.

3. TECHNICAL RESULTS

A study of operational amplifier dc testing resulted in a simplified test circuit for use with ATE which does not need the use of a null-feed-back amplifier. This study also examines the use of a minimum limit approach to open-loop gain testing which would not be suitable for qualification testing (see section III).

Transient response measurement of op amps revealed many ATE-related problems which contribute to inaccuracy and unrepeatability. Some possible approaches to reduce these errors were explored (see section IV).

The testing of linear comparators was accomplished using a new method which does not need a null amplifier and uses no feedback. This testing method and its resulting accuracy is explained in section V. Evaluation of gain tests revealed a possible overstress of the device under certain conditions. Gain testing was modified to reduce the effects of chip heating and increase repeatability.

The responses from users and suppliers to an informal survey confirmed the results experienced with the existing test methods, and supported many of the conclusions reached in this report.

SECTION II

INTRODUCTION

The test methods and specifications for high reliability linear microcircuits are contained in MIL-STD-883 and MIL-M-38510 slash sheets, respectively. There has been concern about measurement accuracy and repeatability of test methods involved with the use of automatic test equipment (ATE). Some of the repeatability problems have been attributed to the greater measurement speed available with ATE and the difficulties using the null-feedback amplifier because of circuit stability. Most of these ATE-related problems fall in the area of test circuit layout and placement of components in association with a null-feedback amplifier. Additionally, the value of open-loop gain measurements has been questioned; chip self-heating can cause nonrepeatability and/or a false negative gain.

The present program was performed to address these ATE-related difficulties. Four preselected linear microcircuits with specific electrical characteristics were tested using ATE and bench test methods. The specific prescribed test requirements and test samples used in this study are contained in Table 1.

TABLE 1. TEST REQUIREMENTS AND SAMPLES

Device Type	Characteristics	Required Tests	Test Samples
LM108A operational amplifier	Very low input offset and bias currents	All dc (static) test requirements in MIL-M-38510/10104 Table III except Delta VIO/Delta T and Delta IIO/Delta T and subgroups 7 and 8 (Transient response)	10 each; Advanced Micro Device (AMD) TO-5, National Semiconductor (NSC) TO-5
LM118 operational amplifier	High speed, wide bandwidth	All transient response tests in MIL-M-38510/10107 Table III subgroups 7,8,12, and 13 only (AC tests).	10 each, AMD TO-5, NSC TO-5
LM111-linear comparator	Low input current - high output current capability	All dc (static) tests in MIL-M-38510/10304 Table III except Delta VIO/Delta T and Delta IIO/Delta T.	10 each; AMD TO-5, NSC TO-5, Texas Instrument DIP
TL061 - Field effect transistor input operational amplifier	Extremely high input impedance	Input leakage currents and settling time parameters in MIL-M-38510/11901	10 each; TI MINI-DIP

Two bench test fixtures, one for the operational amplifiers covered by MIL-M38510/101, the other for the comparator as defined by MIL-M-38510/103, were constructed to evaluate the existing specifications and to provide another source of test data to determine repeatability and accuracy of alternate test methods. These test fixtures also served to expose the layout and construction problems encountered with the null-feedback amplifier circuit.

Following specification evaluation, alternate approaches to the test problem were devised for use on Martin Marietta's Tektronix S-3260 automatic test systems. These proposed test methods, however, were also designed to be applicable to any general-purpose automatic test equipment. In all cases the test circuit design emphasized simplicity and repeatability without the use of a null-feedback amplifier.

A further aspect of this program was an informal industry survey performed to sample the thinking of other microcircuit users and suppliers on the value of these test conditions currently detailed in the MIL-M-38510 slash sheets for linear devices.

The proposed alternate test methods are described in detail in sections III, IV, and V. These sections also discuss repeatability and analysis of the effects of chip heating and soak times. Section VI presents the results of the industry survey. Finally, section VII presents this study's conclusions, along with recommendations for additions to MIL-STD-883 test methods and modifications or additions to the MIL-M-38510 slash sheets.

SECTION III

TEST DEVELOPMENT FOR THE LM108A AND TL061

1. OBJECTIVES

The major objective in this study of testing operational amplifiers (op amps) on ATE was to simplify the testing for static and dynamic tests while maintaining accuracy and repeatability. The following basic requirements had to be met to accomplish this objective:

1 The test circuit as well as the test fixturing should be simple and applicable to generic types

2 The test software had to be relatively simple and easily changeable to meet the requirements of the many different test limit specifications contained in the MIL-M-38510 slash sheets.

2. SUMMARY

A test circuit serving both dc and ac test requirements for MIL-M-38510 would produce test-time savings, as well as significant cost savings in terms of fixture construction. However this is impractical because of the basic incompatibility of the dc ad ac test conditions explained in detail in section IV.

A new test circuit was designed to meet the requirements of Group A, subgroup 1 through 6 testing of MIL-M-38510/101. This circuit had 22 discrete parts, as opposed to the present MIL-M-38510 circuit of more than 30 parts, depending on oscillation suppression requirements. The new circuit uses a modular concept for which parts are readily available. All components are mounted on a standard 40-pin wire-wrap socket (See Figure 1) that is independent of a general-purpose master fixture (Figure 2). The schematic for these fixtures is shown in Figure 3. By separating the master test fixture from the individual test circuit module, versatility is increased and many different part types may be tested with the same master test fixture. Oscillation suppression, if needed, may be applied to each individual module rather than using relays to switch it in and out as done on a single fixture concept.

A test program was generated to meet the needs of general purpose static and dynamic operational amplifier testing. This program could be implemented on any largescale ATE with comparable dc parametric capabilities. The program was designed to be as general as possible so that in most cases only the device specification table had to be changed from one application to another.

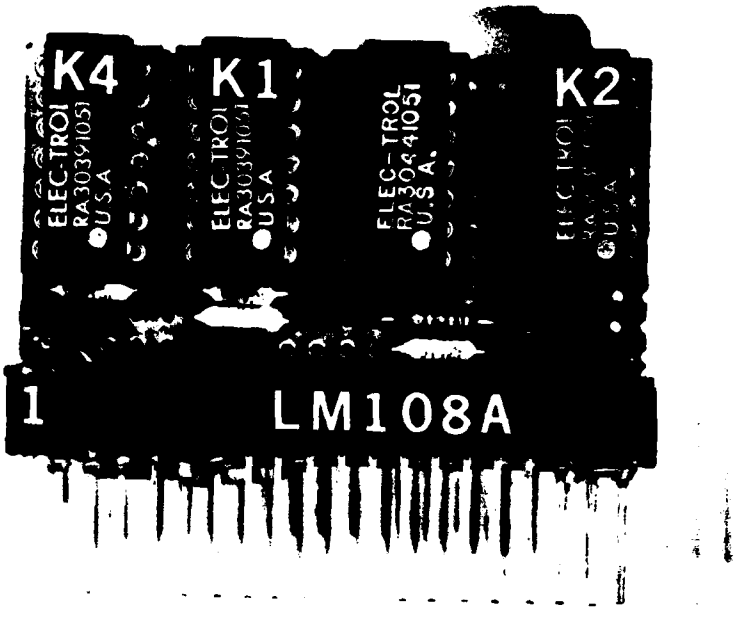

Figure 1. Plug-In for LM108A and TL061
Automatic Test Fixture

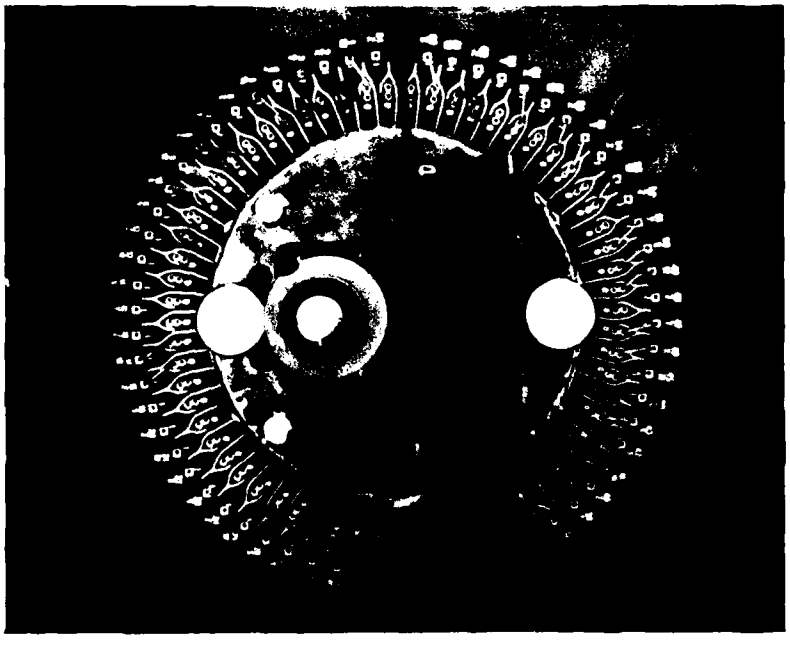

Figure 2. General Purpose DC OP AMP Automatic
Test Fixture

3. CIRCUIT DESCRIPTION

The test circuit for this evaluation (Figures 3 and 4) is a modified version of the circuit found in MIL-STD-883B Method 4001, Figure 4001-1. R1 and R3A are chosen to give a loop gain of approximately 1000 with K3 in position 1. R2 and R3B result in a loop gain of approximately 100 with K3 in position 2. The loop is utilized in op-amp testing only to amplify the minute values to be measured. Therefore, the fact that the gain of the circuit is not exactly 1000 or 100 is relatively unimportant, as long as the actual gain of the loop is known when a measurement is made.

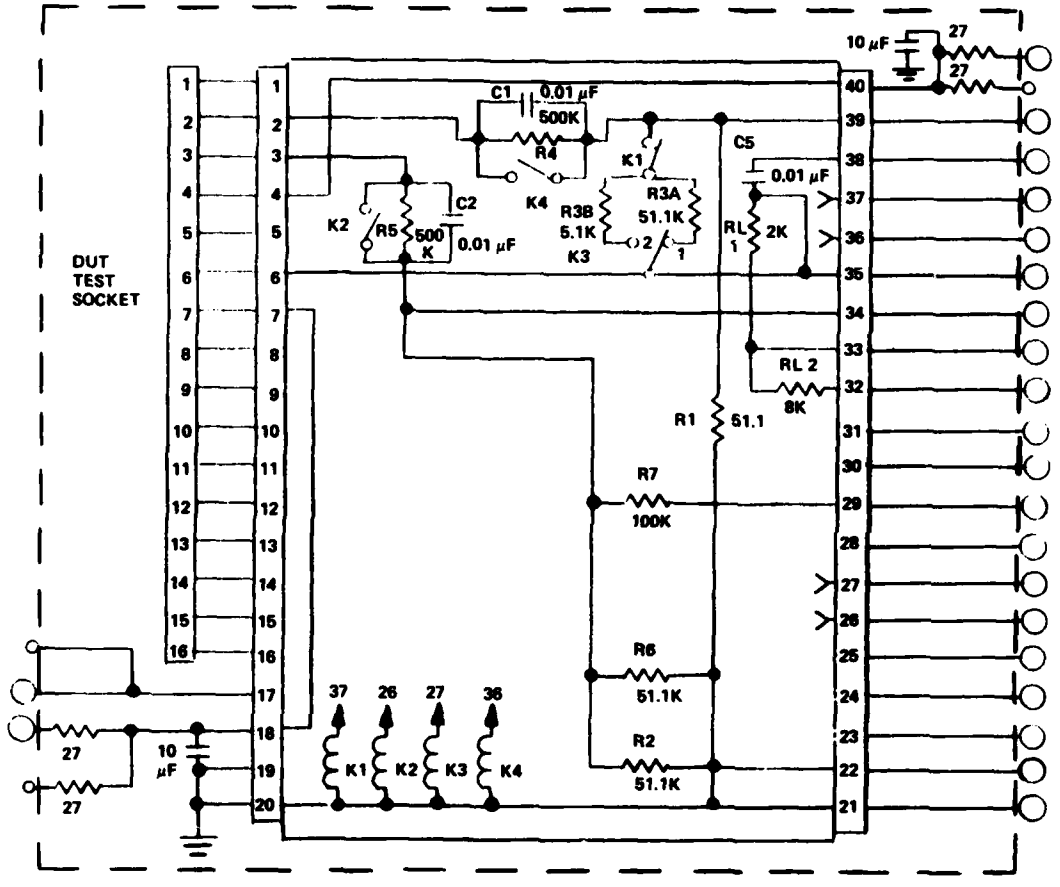

Figure 3. Component Schematic for General Purpose DC OP AMP Test Circuit with Plug-In

Since it is unimportant to have a precise loop gain, standard 1-percent resistors may be used. The gain of these resistors is measured by an external ohmmeter at the time of fixture construction and then used by the test program to calculate actual loop gain. The circuit is verified prior to any device testing by utilizing the ATE to measure loop-related resistors to an accuracy of 1 percent of the value measured by the external ohmmeter. This test not only

ensures that the test module has been correctly inserted into the master fixture, but also checks circuit relays for operation, indirectly providing some assurance that the ATE is operational prior to test.

Resistors R2 and R6 are used to balance the positive input of the differential op amp. The value of R6 was chosen for optimum balance of the op amp with K3 (Figure 4) at position 1 (where loop gain ≈ 1k). All static measurements within the maximum limits specified in MIL-M-38510/101 for the LM108A result from the test circuit being in this configuration (i.e. K3 in position 1). The only exceptions were for the TL061 in which VIO measurements, where VCM is not equal to 0.0V and VIO is greater than 1 mV, were the only parameters that used the gain of the 100 loop configuration. When the loop gain is 100, one additional measurement error is induced. Further loop gain error, although negligible, is induced due to the imbalance of the DUT caused by the improper value of R6. This error could be eliminated through the use of DPDT relay at K3 which would switch in differing values for R6 as well as R3.

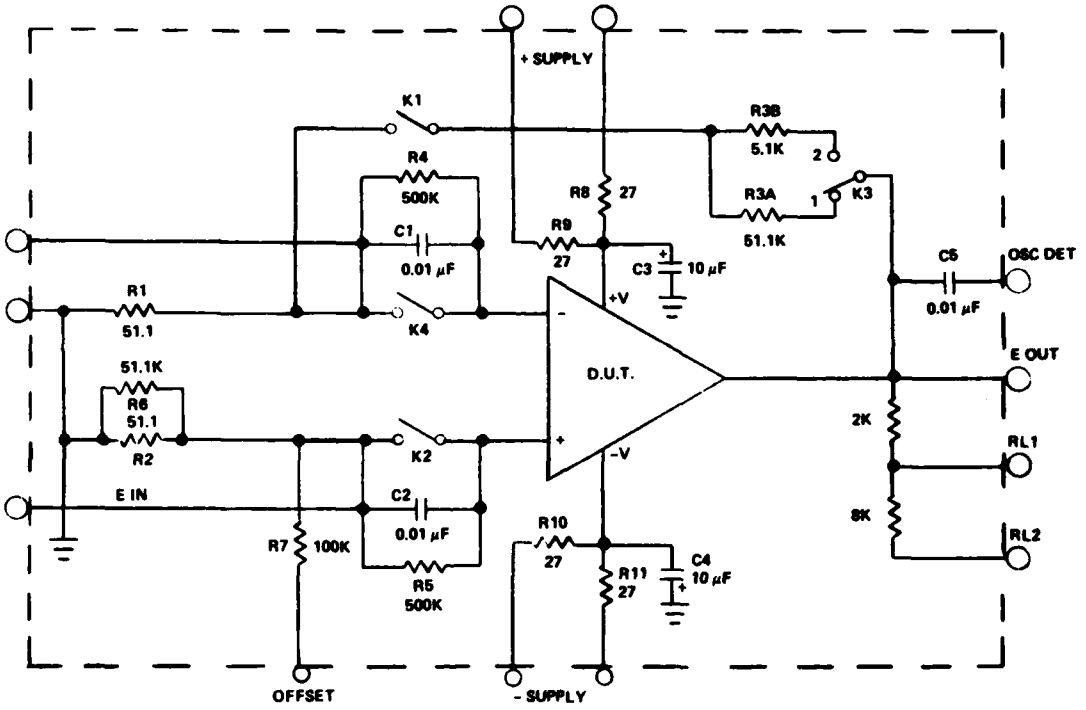

Figure 4. General Purpose DC OP AMP Test Circuit

With the addition of R7, R2 and R6 form part of a voltage divider used to null the op amp for measurements other than VIO. The resistors were measured at fixture construction with an external ohmmeter and the values used in the test program to calculate the ratio of the OFFSET divider.

Resistors R4 and R5 sense input bias currents, then the resultant voltage drop is amplified and measured at the op amp output. The values of both R4 and R5 are chosen so that the maximum voltage at the output of the circuit is 1V at the maximum specified IIB limit with K3 in position 1 (loop gain ≈ 1K). This keeps the range of the dc measurement system at or below the 1V range for optimum accuracy and resolution of the measurement. Op amp loading is attained by grounding either RL1 for a 2KΩ load or RL2 for a 10KΩ load. Resistors R9 and R10 in conjunction with C3 and C4 form a power supply isolation-decoupling network.

There is limited accuracy for most ATE high-current measurement options because of limited resolution. Separate power inputs are supplied to the device under test, one is used to supply power and one used to measure supply current. The low level supply current measurements are made via R8 and R11. The two resistors serve the same purpose as R9 and R10 and form part of the test circuit only during supply current measurements. Capacitor C5 is used to ac couple the output of the op amp to a comparator in the ATE to detect possible circuit oscillation during test.

4. GAIN PARAMETER STUDIES

Using the new test circuit (Figure 4), two approaches were investigated to evaluate open-loop gain measurements for operational amplifiers. One approach is the go/no-go measurement. This method is used to test the DUT for minimum gain as specified in MIL-M-38510/101F, Table III.

The first step in either approach requires that the op amp be nulled to zero output. To null the op amp input offset voltage, a voltage equal to -(VIO((Rx + R7)/Rx)), where Rx = R2 and R6 in parallel, is applied to the sample device via the OFFSET node.

Since gain per MIL-M-38510/101F is measured with the output of the DUT at ±15 volts, minimum gain is tested using the following procedure. A voltage equal to 15 divided by the specified minimum open-loop gain multiplied by the offset divider (Ein) is either added to or subtracted from the voltage being applied to the OFFSET node. The resulting voltage is measured at EOUT. If the resultant voltage at EOUT is greater that 15 volts, the operational amplifier has an open-loop gain of greater than or equal to the minimum specified.

The second approach takes the go/no-go test one step further. With this method, testing for gain is arbibrarily begun at five times that specified as minimum. If the resultant voltage at EOUT $\geq$15, the gain is equal to or greater than five times the minimum. If the voltage at EOUT is less than 15, the gain expected is lowered by a fixed amount and the test sequence is repeated until EOUT $\geq$15 volts. The point at which EOUT $\geq$15 is where minimum gain is calculated: AVOL = EOUT/EIN.

Obviously, the first approach (go/no-go) is faster and probably sufficient for most applications. Knowledge of the precise value of open-loop gain in the present MIL-M-38510/101 is not required except for qualification. MIL-M-38510 includes reliability oriented tests, which is not a significant factor here.

5. MEASUREMENT ACCURACY OF LM108A AND TL061

The accuracy of any measurement, whether it be on the bench or on ATE, is dependent on the test circuit design, the accuracy, and the resolution of the measuring instrument. Accurate high-resolution test equipment is ineffective if the op amp under test is oscillating because of unstable test circuit conditions. The circuit shown in Figure 4 has been found to be extremely stable for not only the LM108A and TL061 evaluation, but also for a variety of other op amp types that were evaluated. Although not required by this study, a quantity of M118 and LM2101 were tested using the same test circuit with only the values of R4 and R5 changed to facilitate biascurrent measurements. Lots of more than 500 LM118 samples and 1200 LM2101 samples were tested using the test circuit of Figure 4 with no indication of test circuit instability. Delta VIO and Delta IIB were measured and calculated by the ATE after 168-hour burn-in; both indicated very favorable repeatability.

Since the majority of the static tests for the LM108A and TL061 use the closed-loop configuration as does the existing MIL-M-38510 circuit, accuracy of these tests is dependent on three factors:

1 The accuracy of R1 and R3, which determines circuit-loop gain

2 The accuracy of R4 and R5 which senses input-bias current

3 The accuracy of the ATE dc measurement system.

The methodology of the test and therefore the measurement equations remain essentially the same as MIL-M-38510 only without the null amplifier. Table 2 describes the conditions and equations for the parameters investigated.

General instrumentation error calculations are usually complex calculations rather than simple additive errors. Worst case error will be established by adding worst case circuit error and worst case dc measurement system error.

For VIO measurements, we need to be concerned with the accuracy of R1 and R3 with a worst-case error of less than 0.1 percent when measured with an ohmmeter having accuracy greater than 0.1 percent. The second cause for error for VIO measurements is the dc measurement system. Worst-case error for a VIO measurement of 1 mV using the new ATE circuit (Figure 4) can be defined as follows:

$$VIO = \frac{EOUT}{(R1 + R3/R1)}$$

where loop gain = $\approx$ 1K.

The equation for nominal gain calculated for measured values of R1 = 51.1Ω and R3 = 51.1KΩ is:

$$\frac{R1 + R3}{R1} = \frac{51.1 + 51{,}100}{51.1} = 1001$$

TABLE 2. TEST TABLE FOR LM108A USING TEST CIRCUIT OF FIGURE 4.

PARAMETER	EOUT	SUPPLY VOLTS +	SUPPLY VOLTS -	RELAY K1	RELAY K2	RELAY K3	RELAY K4	LOAD RL1	LOAD RL2	EQUATION	SPEC LIMIT WORST CASE ACCURACY	RESOLUTION
VIO	E1	35	-5	↑	O	2/	O	↑	↑	VIO = EOUT/((R1 + R3)/R1)	0.70% 5/ 2.35% 4/	0.05 μV 7/ 5/ 0.5 μV 6/ 5/ 0.5 μV 7/ 4/ 5 μV 6/ 4/
	E2	5	-35	|	P	2/	P	|	|			
	E3	20	-20	|	E	2/	E	|	|			
	E4	5	-5	C	N	2/	N	|	|			
+IIB	E5	35	-5	L	C	1	|	O	O	+IIB = (EOUT/((R1 + R3)/R1))/R5 1/	0.70% 5/	0.1 pa 7/ 5/ 1 pa 6/ 5/
	E6	5	-35	O	L	1	|	P	P			
	E7	20	-20	S	O	1	|	E	E			
	E8	5	-5	E	S	1	↓	N	N			
-IIB	E9	35	-5	D	E	1	C	↑	↑	-IIB = (EOUT/((R1 + R3)/R1)/R41/		
	E10	5	-35	|	D	1	L	|	|			
	E11	20	-20	|	•	1	O	|	|			
	E12	5	-5	↓	↓	1	D	↓	↓			
IIO	CALCULATED USING +IIB AND -IIB MEASUREMENTS									IIO = +IIB - (-IIB)	14%	
+PSRR	E13	10	-20	↑	↑	2/	↑	↑	↑	+PSRR = ((E3-E13)/LOOP GAIN) x 10^5	0.7% 5/ 2.35% 4/	SAME AS VIO IN μV/V
-PSRR	E14	20	-10	C	O	2/	O	|	O	-PSRR = ((E3-E14)/LOOP GAIN) x 10^5		
CMRR	E15	35	-5	L	P	2/	P	|	P	CMRR = 20 LOG $\left\lvert 30\left(\frac{E15-E16}{\text{LOOP GAIN}}\right)\right\rvert$	0.7% 5/ 2.35% 4/	4.34x10-4db6/4/ 4.34x10-6db7/5/
	E16	5	-35	O	E	2/	E	|	E			
+IOS	IOS	15	-15	S	N	1	N	O	N	+IOS = IOS EIN = +50 MV	+/- 0.7%	5 μa
-IOS	IOS	15	-15	E	|	1	|	P	|	-IOS = IOS EIN = -50 MV		
ICC	ICC	15	-15	|	|	1	|	E	↓	ICC = ICC	+/- 0.9%	0.5 μa
+VOP	E17	20	-20	|	|	1	|	N	G	+VOP = EOUT EIN = +50 MV	+/- 1.4%	5 mV
-VOP	E18	20	-20	↓	|	1	|	↓	O	-VOP = EOUT EIN = -50 MV		
AVOL	E19 E20	20	-20	OPEN	|	|	↓	↓	N D	AVOL = EOUT/EIN 1/ 3/	NA	NA

NOTES:
1/ EOUT SET TO 0 ±50 MV PRIOR TO TEST VIA OFFSET INPUT
2/ R3 = EITHER R3A OR R3B VIA RELAY K3. THE POSITION OF K3 IS SELECTED TO GIVE OPTIMUM ACCURACY AND RESOLUTION AT EOUT.
3/ E19 = (EOUT WITH EIN = 15)/MINIMUM GAIN
E20 = (EOUT WITH EIN = -15)/MINIMUM GAIN
4/ R3 = R3B (LOOP GAIN ≈100)
5/ R3 = R3A (LOOP GAIN ≈ 1K)
6/ MEASUREMENT SYSTEM 1 VOLT RANGE
7/ MEASUREMENT SYSTEM 0.1 VOLT RANGE

where worst-case 0.1 percent measurement accuracies for R1 and R3 are used in the equation, worst-case loop gain can be calculated to be:

$$\frac{R1MIN + R3MAX}{R1MIN} = \frac{51.0489 + 51151.1}{51.0489} = 1003.$$

Thus worst-case loop error due to the measured inaccuracies of R1 and R3 can be calculated to be:

$$\frac{\text{Worst-Case Loop Gain - Nom Loop Gain}}{\text{Nom Loop Gain}} \times 100\% = \frac{1003 - 1001}{1001} \times 100\% = 0.2\% \text{ error}$$

where loop gain $\approx$ 100

$$\frac{R1NOM + R3NOM}{R1NOM} = \frac{51.1 + 5110}{51.1} = 101.0$$

$$\frac{R1MIN + R3MAX}{R1MIN} = \frac{51.0489 + 5115.11}{51.0489} = 101.2$$

$$\frac{\text{Worst-Case Loop Gain-Nom Loop Gain}}{\text{Nom Loop Gain}} = \frac{101.2 - 101.0}{101.0} \times 100\% = 0.198\% \text{ Error}$$

Using the Tektronix S-3260 dc measurement system, the range required for a 0.5 millivolt VIO measurement is 1 volt (0.5 mv x 1000 (loop gain) = 0.5V). The measurement system 1-volt specification is 0.1 percent of value plus 2 millivolts. Therefore, a dc measurement system error of 2.5 mV is possible.

The total worst case measurement error for a loop gain configuration of approximately 1000 is $\pm$0.2 percent loop resistor error adding a 2.5 μV $\left(\frac{2.5\text{ mV}}{\text{loop gain}}\right)$ dc measurement system error. The total 0.5 mV VIO measurement error is 0.7 percent. The calculation changes when using a loop gain of approximately 100. Now the dc measurement system (100 mV range) specification error is 0.015 percent of value plus 1 MV, resulting in a possible measurement error of 1.075 mV. Worst case measurement error for a loop gain of approximately 100 is $\pm$0.2 percent plus 10.75 μV $\left(\frac{1.075\text{ mV}}{\text{loop gain}}\right)$ measurement system error, for a total worst case error of 2.35 percent for the 0.5 mV VIO measurement.

When VIO measurement at VCM, (other than 0V,) exceeds 1 mV (1V at EOUT), as with the TL061, it is important during program generation to maintain a loop gain configuration of approximately 100. This prevents the output of the DUT from going to either positive or negative rail causing erroneous readings.

One additional error in IIB measurements, that of R4 and R5, is of interest. This error was determined to be less than 0.1 percent with the use of an external ohmmeter. The total worst case error for a calculated IIB measurement of 2 nA where

IIB = ((V1 - V2)/loop gain)/RS

is as follows:

1. V1 is defined as EOUT with both K2 and K4 closed and the output set to 0.0V ± 50 mV via the offset input on the test circuit (Figure 4)

2. V2 is EOUT with either K4 or K5 open, and RS is the measured value for either R4 or R5

3. V1 (error) = 0.15% (EOUT) + 1 mV (100 mV range)

4. V1 is offset to ±50 mV, so worst case V1 (error) = 0.15 percent (50 mV) + 1 mV or 1.075 mV.

V2 (error) which equals 0.1 percent (EOUT) + 2 mV (1V range). EOUT will equal 1V for an IIB of 2 nA, therefore worst case, V2 (error), is equal to 0.1 percent (1V) + 2 mV or 3 mV. Total worst case error, V1 (error) + V2 (error), is equal to 4.075 mV at EOUT or approximately 8.15 pA with RS ≈ 500K and loop gain ≈1000.

Adding the constant 0.2 percent worst case loop error for VIO and 0.1 percent constant worst case RS measured values, calculated worst case total IIB measurement error is specified as ±0.3 percent of reading plus 8.15 pA. This is approximately 0.7 percent for a measurement of 2 nA.

The accuracy error for IIO is calculated from the basic equation,

IIO = +IBB - (-IIB),

and is the same method used in MIL-M-38510/11901 for calculating IIO. Different full scale limits are applicable for IIO and IIB. Therefore, the calculated worst case accuracy error for a calculated IIO of 200 pA is:

$$\text{IIO ERR} = \text{IIBERR} \frac{((\text{MaxIIB+}) + (\text{MAXIIB-}))}{\text{MAXIIO}}$$

$$= 0.14 = 0.007 \frac{(2\text{ nA} + 2\text{ nA})}{0.2\text{ nA}}$$

Worst case IIO (error) = 14 percent, MAXIIB is the maximum specified IIB limit and MAXIIO is the maximum specified IIO limit.

Power supply rejection ratio (PSRR) measurements rely on the same circuit configuration as does V10, therefore the same accuracy calculation applies. When measuring the power supply rejection ratio using the new ATE circuit, the following formula applies:

$$PSRR = ((V1 - V2)/\text{LOOP GAIN}) \times 10^5$$

For a positive PSRR measurement, V1 = EOUT with +VCC = +20V and - VCC = -20V and V2 = EOUT with + VCC = +10V and -VCC = -20V. For a negative PSRR measurement, V1 = EOUT with +VCC = +20V and -VCC = -20V. V2 = EOUT with +VCC = +20V and -VCC = -10V.

Common mode rejection ratio (CMRR) with the ATE circuit is calculated as:

$$CMRR = 20 \text{ LOG } |30((V1 - V2)/\text{LOOP GAIN})|$$

where V1 = EOUT measured at a common mode voltage of +15V and V2 = EOUT measured at a common mode voltage of -15V. Common mode is achieved by shifting the values of the plus and minus power supplies rather than applying an external voltage. Since the common mode condition is created within the DUT rather than through external application via R_1 and R_2, critical matching of these resistors becomes unnecessary. The measurement accuracy calculation is the same as VIO.

The accuracy of the IOS measurement is a direct measurement unaffected by the loop and is derived strictly from the dc measurement specification. In the case of the LM108A with a maximum specified IOS of 15 ma, accuracy for a reading of 10 ma would be determined as $\pm$0.5 percent of reading +20 µa or $\pm$0.7 percent.

The accuracy of the ICC measurement can also be derived directly from the dc measurement specification. In the case of the LM108A with a maximum specified ICC of 600 µa, accuracy would be $\pm$0.5 percent of reading $\pm$2 µa which, for a reading of 500 µa, would be accurate $\pm$0.9 percent.

VOP accuracy, another parameter that is directly measured, is determined from the ATE's dc measurement specification. For the LM108A with a nominal voltage swing of $\pm$18V, the measurement accuracy would be $\pm$0.3 percent of reading +200 mV or $\pm$1.4 percent.

6. REPEATABILITY - LM108A AND TL061

Bench-type measurements typically involve the use of scopes, power supplies, digital voltmeters, and external components such as resistors, capacitors, switches, relays, and nulling amplifiers. There are numerous variables involved with this whether between devices during a single setting or between test set ups. These variables can be attributed to human error in reading and interpreting meters, and to equipment-induced errors derived from power supply drift, calibration accuracy, and differences between two similar pieces of equipment used for the same purpose from one test to the next.

With automatic tests, these variables are reduced. The use of differential voltage measurements during automatic test increases accuracy and resolution. An automatic test can be selfchecking. Before any test is made, a calibration check can be performed in a few seconds to ensure stability of the system.

A repeatability study was performed using 10 TL061 and 20 LM108A operational amplifiers. All static parameter requirements with the exception of Delta VIO and Delta IIB were studied for the LM108A. The TL061 was used to determine VIO and IIB repeatability. Test results are summarized in the following paragraphs.

Figure 5 is a typical shmoo plot representation of 20 measurements VIO at VCM = -15V for LM108A. Measurements 1 through 10 were successive measurements done on one Tektronix S3260, and measurements 11 through 20 were successive measurements done on another system of the same type. Measurements ranged between 283 μV and 292 μV for a calculated variation of approximately 3 percent.

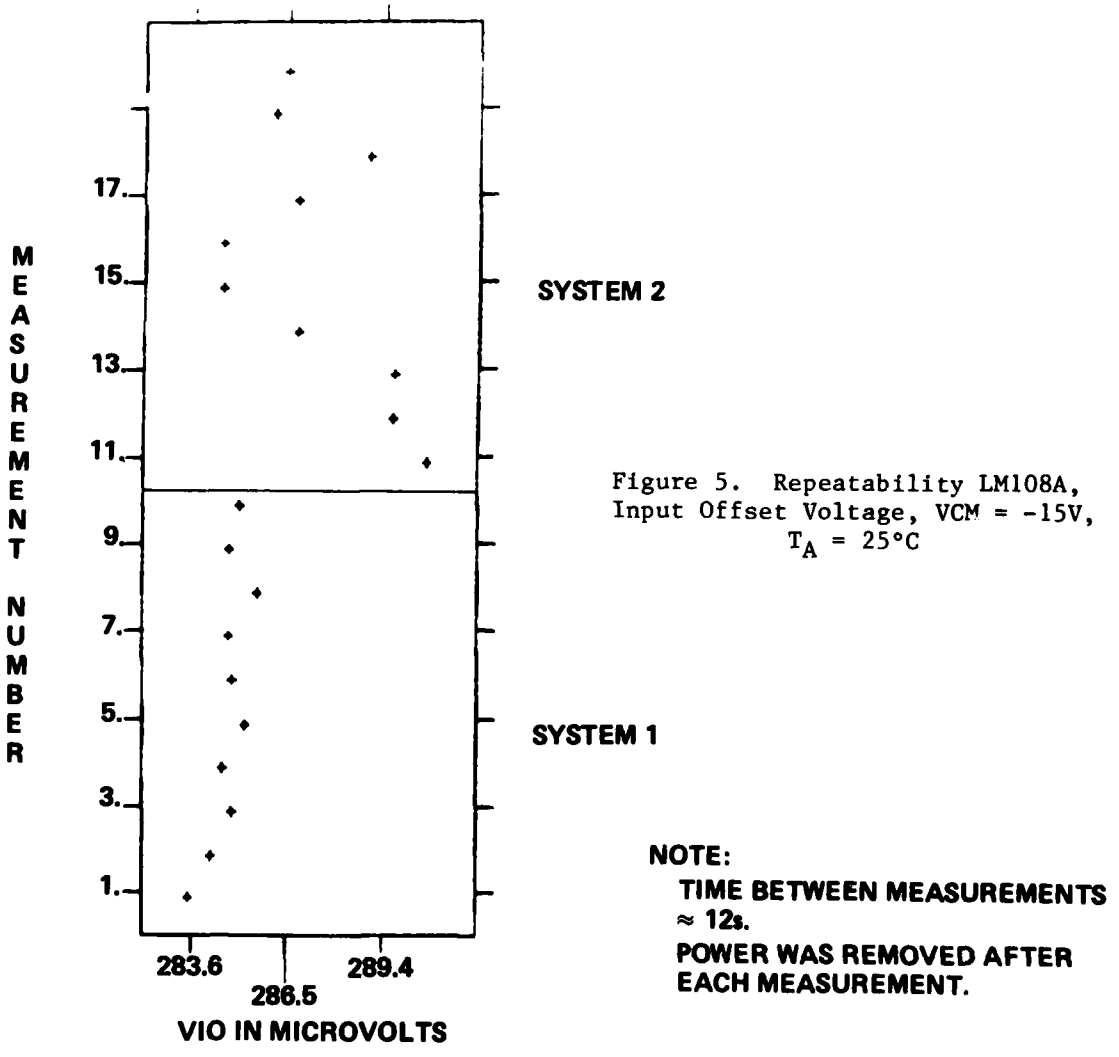

Figure 5. Repeatability LM108A, Input Offset Voltage, VCM = -15V, T_A = 25°C

Figure 6 represents the same measurements taken with VCM = 0. Measurements ranged between 347 μV and 355 μV for a calculated variation of 2.2 percent.

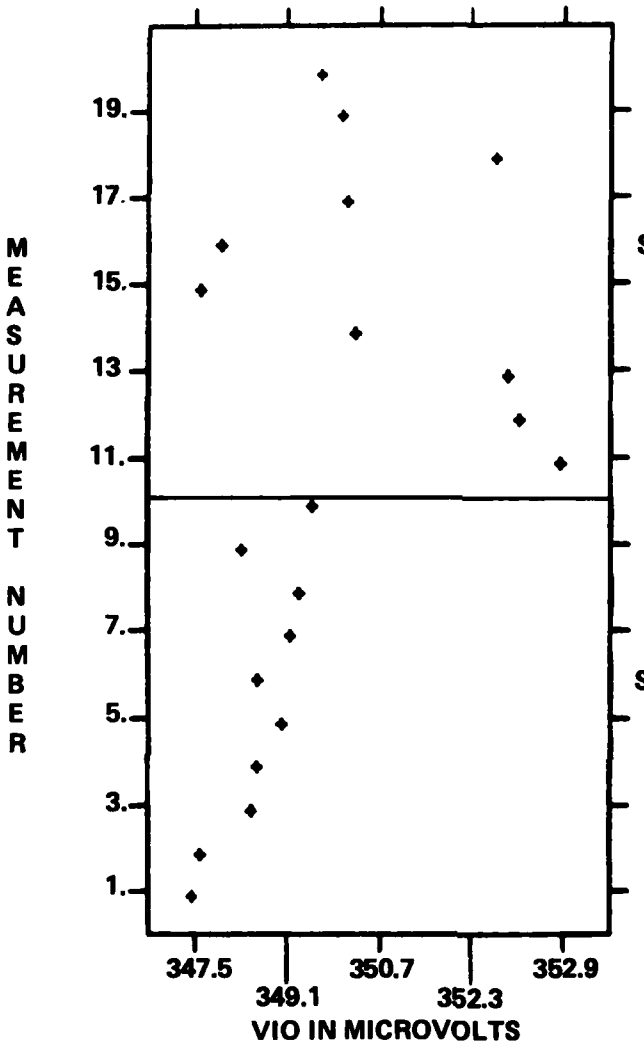

Figure 6. Repeatability LM108A, Input Offset Voltage, VCM = 0.0V
T_A = 25°C

NOTE:
TIME BETWEEN MEASUREMENTS ≈ 12s.
POWER WAS REMOVED AFTER EACH MEASUREMENT.

Figure 7 represents typical-IIB measurements at a VCM of 0 volt for TL061. Again, measurements 1 through 10 were performed sequentially on the Tektronix S3260, and measurements 11 through 20 sequentially on another system of the same type. Measurements ranged between 9.1 and 9.9 picoamps for a calculated variation of approximately 8 percent. If we consider an accuracy calculation of ±0.7 percent of maximum spec (200 pa·), we are well within the ±1.4 picoamp accuracy allowed.

Figure 8 represents measurements of all 20 LM108A op amps for calculated values of IIB. Each point on the shmoo plot represents the percent of error of 10 IIO measurements taken ≈ 12 seconds apart on the same part. To show

repeatability between ATE and bench, 9 of these 10 measurements were taken with the new ATE circuit, the tenth measurement was taken on the bench using the present MIL-M-38510 test circuit. The results of this bench measurement were then entered into the computer via keyboard. Both bench and ATE measurements were within a 5 percent repeatability of each other. The highest and lowest of these 10 data points were used to calculate the repeatability error per the following:

Percent Repeatability Error = (highest reading - lowest reading)/max limit x 100 percent.

Figure 9 represents VIO measurements for all 10 TL061 op amps in the test lot. The means of data acquisition and percent of error calculation are the same as described for the 20 LM108A op amps. Figure 10 represents IIO data for TL061, and because of the extremely low absolute values (<9 pa), the percent of repeatability error is significantly higher than that of previous data.

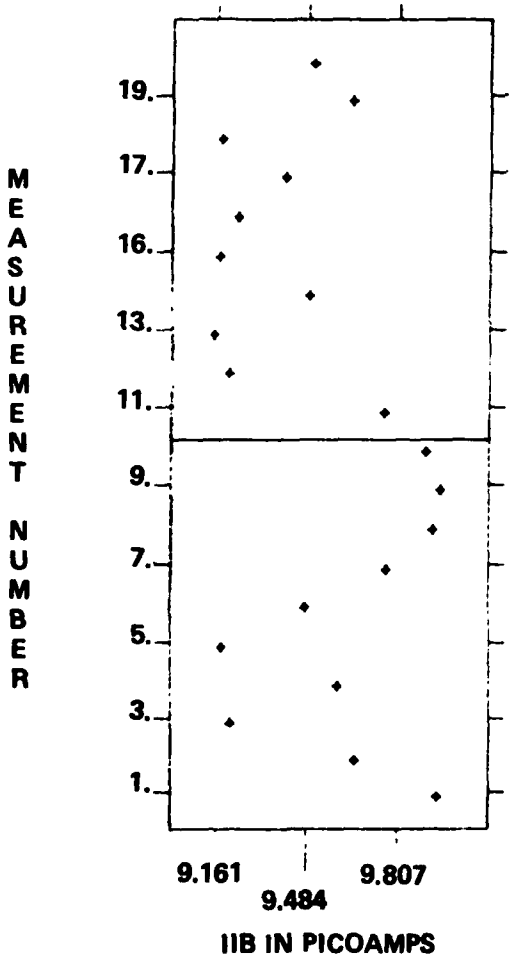

Figure 7. Repeatability TL061, -Input Bias Current, VCM = 0.0V
T_A = 25°C

NOTE:
TIME BETWEEN MEASUREMENTS ≈ 10s.
POWER WAS REMOVED AFTER EACH MEASUREMENT.

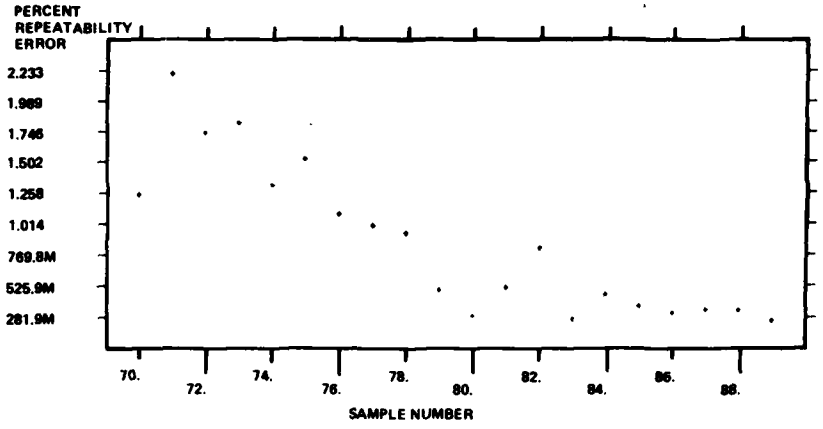

Figure 8. Input Bias Current, Percent Repeatability versus Sample Number for the LM108A, VCM = 0.0V, T_A = 25°C

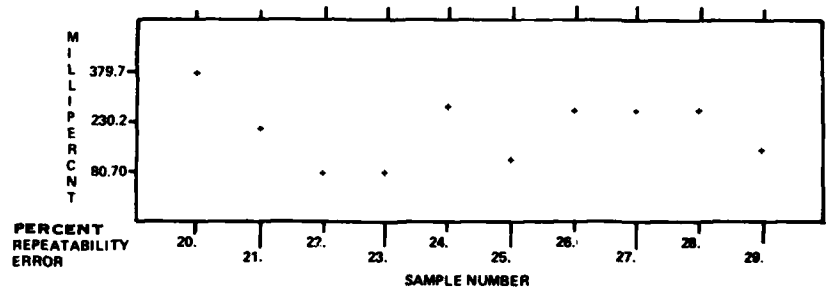

Figure 9. Input Offset Voltage, Percent Repeatability versus Sample Number for the TL061, VCM = 0.0V, T_A = 25°C

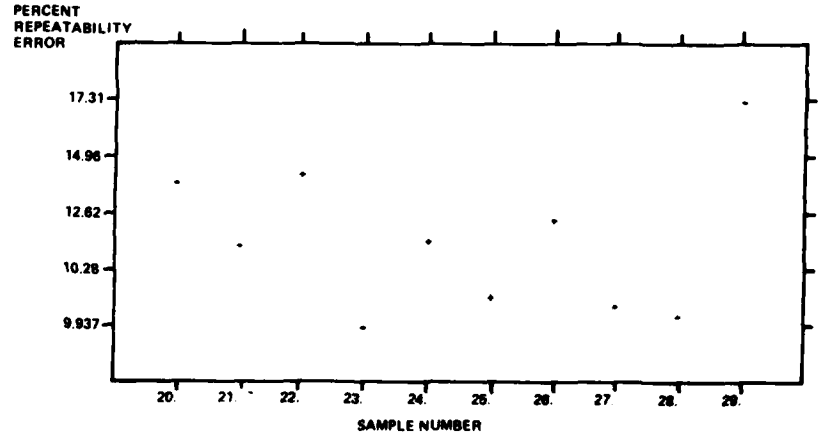

Figure 10. Input Offset Current, Percent Repeatability versus Sample Number for the TL061, VCM = 0.0V, T_A = 25°C

7. CHIP HEATING - SOAK TIME FOR LM108 AND TL061

Figure 11 represents percent of repeatability versus soak time for VIO measurements for a typical TL061 op amp in the test lot. Each point shows the average percent of repeatability versus soak times before measurements were taken. Left of zero soak times are measurements taken with DUT power turned off between tests allowing the test circuit to stabilize prior to DUT measurement. Right of zero soak times are measurements taken with the power applied continuously to the DUT. Figure 12 represents the same type of data for LM108 VIO measurements. There is no significant change in percent of error where DUT power is applied continuously; however as power off time is increased, percent of error increases indicating a change due to thermal heating effects.

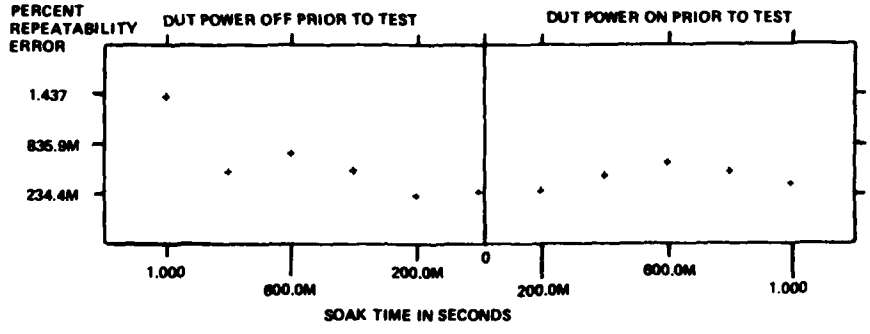

Figure 11. Soak Time versus Percent Repeatability for the TL061 Measuring Input Offset Voltage, VCM = 0.0V, T_A = 25°C

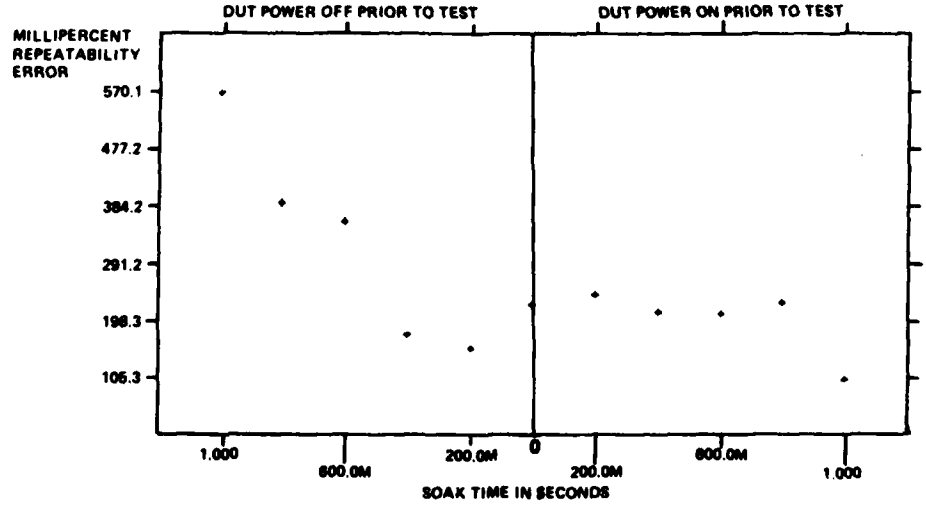

Figure 12. Soak Time Versus Percent Repeatability for the LM103A Measuring Input Offset Voltage, VCM = 0.0V, T_A = 25°C

Figure 13 shows a typical IIO repeatability error for TL061 peculiar to IIB measurement with the ATE circuit. The settling delay is due to the integration effect of capacitors C_1 or C_2. At 10 pA of current, between 100 and 500 ms are required to fully charge the 0.01 µF capacitor to the equilibrium value IR drops across the 500 kΩ resistor (R4 or R5) of 5 µV.

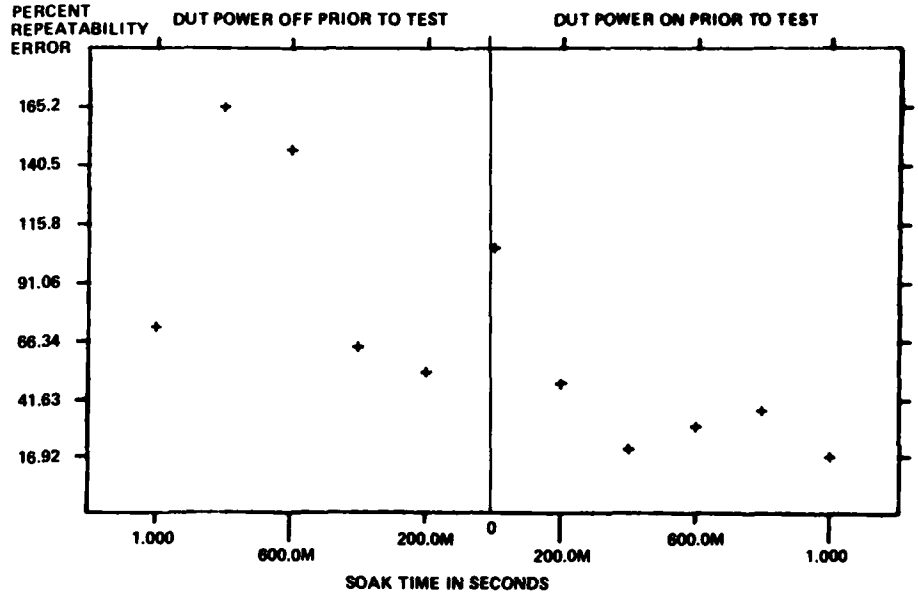

Figure 13. Soak Time versus Percent Repeatability for the TL061 Calculated Input Offset Current, VCM = 0.0V, T_A = 25°C

SECTION IV

TEST DEVELOPMENT FOR THE LM118 AC PARAMETERS

1. OBJECTIVE

The transient response tests for the LM118 operational amplifier are described in MIL-M-38510/101. These tests are rise time, overshoot, and bandwidth at a 50 MV input signal level, also slew rate and settling time at a ±5.0V input signal level. The problems involved with the use of this test circuit are its inherent instability due to the lack of external frequency compensation, and the millivolt signal levels that are not compatable with general purpose ATE. The objectives of this effort were to:

1. Investigate the possibility of combining the transient response tests on the same test fixture (Figure 4) developed for use on the LM108A operational amplifier, discussed in Section III.

2. Investigate the automatic test-related variables with the use of the existing transient response test circuit in MIL-M-38510/101.

3. Develop new test methods to perform the transient response tests with repeatable, accurate results on general-purpose automatic test equipment.

2. SUMMARY

Two test methods were designed for this report. The first approach was to combine the transient response tests and the dc tests on the same test fixture. This approach would reduce test costs due to construction of only one test fixture, and reduction of handling and temperature soak time by a factor of two. This evaluation showed that combination of these two test fixtures into a single unit is not feasible. The need for numerous circuit elements for the dc tests creates many areas of stray capacitance and inductance, causing instability and oscillations. In the input circuit the additional stray capacitance slows down the response time and invalidates the measurement.

The second investigation was to reproduce the existing MIL-M-38510/101 transient response circuit and interface it to the Tektronix S3260 test system. An input attenuator was used to reduce the pulse input by a factor of 100:1 to get a input 50 mV pulse. There were two major difficulties encountered in this approach. First, the 50K source impedance created an unacceptable time constant with the fixture capacitance. This resulted in a false failure of output rise time due to the RC time constant at the input of the device under test.

Second, typical ATE measurement system comparators are not designed to handle millivolt level signals. On the lowest range, 5 volts, the programming accuracy (Tektronix S-3260) is only ±(0.166 percent of value +1 percent of range), while the resolution is 1.67 mV. Although the resolution is good, the accuracy for a 50 mV comparator level is ±50.083 mV, which is unacceptable.

Several methods were explored to minimize ATE-related problems and show improvements in accuracy and repeatability. The final conclusion is that transient response tests cannot be performed wihout extensive fixturing on general purpose ATE.

3. TEST DEVELOPMENT

Based on the problems encountered with the existing transient response circuit, a new test method was developed. The new circuit and fixture (Figure 14 and 15) is similar to that in MIL-M-38510/101 with the following exceptions:

1. The source impedance was reduced from 50KΩ to 10KΩ , giving more circuit layout flexibility by reducing the effect of input stray capacitance. Note: The 50KΩ value was an error in MIL-M-38510/101 and has since been corrected to 5KΩ.

2. The output signal is amplified by a high-speed op amp (LH0032 buffer circuit) to increase the measured output signal to an acceptable level for more accurate measurement.

In this configuration, the gain of the output stage had to be limited to 4:1 to preserve the frequency response of the buffer circuit. With this gain configuration, the repeatability is still not within the 5 percent requirements due to the inaccuracy of the test system comparators. This inaccuracy is reduced somewhat by a comparator calibration technique that was implemented in the software test program. This method uses the comparator to make the zero and 100 percent measurement of the high and low output levels that are about 200 MV and 0.0V, respectively, after amplification. For rise time measurement the adjusted 10 and 90-percent compared levels are then calculated from these values. Thus the inaccuracy is reduced by removing the effect of the comparator offset from the measurement. Using this technique, accuracy is improved by removing the effect of buffer offset, driver offset, and comparator offset. The repeatability is still affected by the single shot time subsystem and the ability of the system to repeat these settings (see subsections 5 and 6).

4. CIRCUIT DESCRIPTION

The test circuit for use with ATE is shown in Figure 14. The device under test is connected in a noninverting gain of 1 configuration. Resistors R1 and R2 provide input attenuation to provide a 50 MV input signal to the test device from the test system drivers. A LH0032 high-frequency amplifier is connected to the output of the device under test to increase the level of the output signal from 50 MV to 200 MV to aid the test system comparator resolution for time measurements.

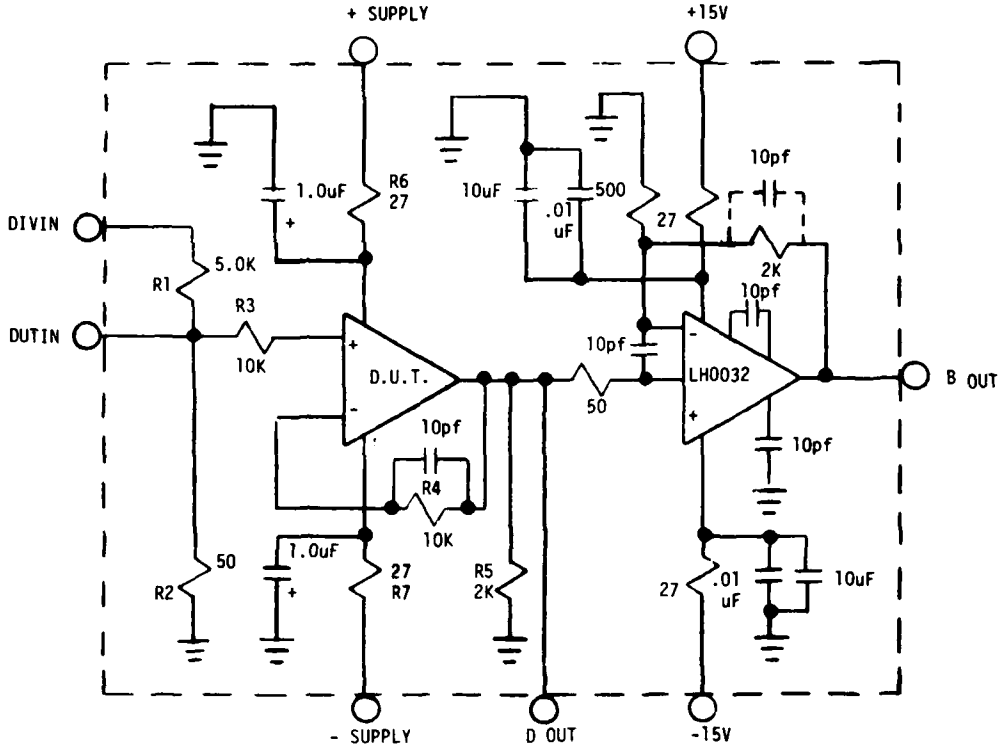

Figure 14. Automatic Test Equipment Operational Amplifier Transient Response Test Circuit

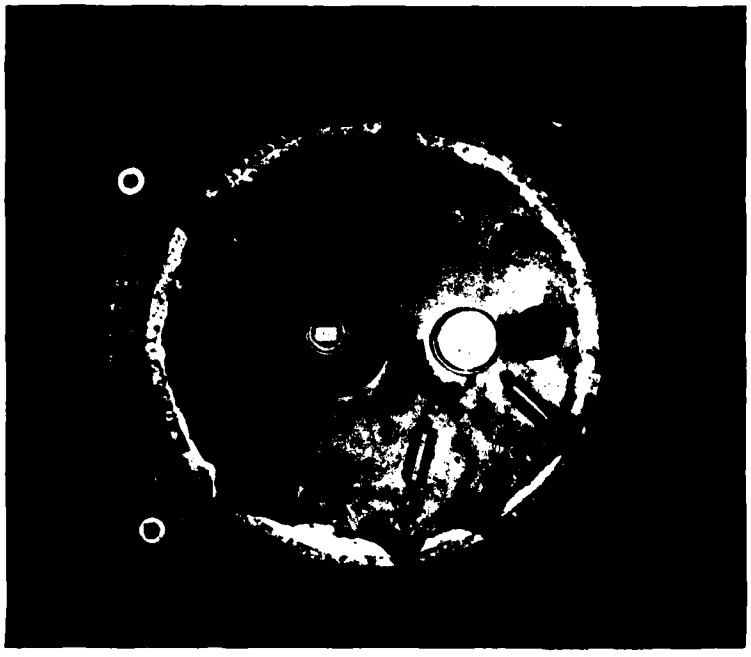

Figure 15. LM118 Fixture for Automatic AC tests on Tektronix S-3260

5. TEST PARAMETERS AND ACCURACY FOR THE LM118

During the rise time test a 5.0V pulse is applied at terminal DIVIN (Figure 14). The output pulse of the DUT is then amplified by the LH0032 buffer. Due to the limited accuracy of the test system comparators, [±0.166 percent of value +1.0 percent of range] on the Tektronix S-3260 test system, a software calibration technique was used in the device test program. The high and low levels of the buffer output (BOUT) are determined by the dc measurement system to assure that the DUT and buffer are functional and to prevent erroneous measurement. These same levels are then determined by the same comparator calibration technique.

The rise time of the buffer amplifier circuit is approximately 5 ns, which will contribute an error of 2.9 percent to 0.75 percent for rise time measurements of 20 ns to 40 ns, respectively. Since the buffer rise time is a constant, the true value can be calculated in the automatic test program as follows:

$$Tr\ (Actual) = \sqrt{Tr\ (Measured) - Tr\ (Buffer)}$$

The following error calculations will assume that this measurement value is corrected in the test program. Comparator level accuracy for the Tektronix S-3260 with MIL-M-38510/101 test conditions is as follows:

$$\begin{aligned} &\pm[0.00166\ (50\ MV) + .01\ (5V)] \\ &= \pm(0.083\ MV + 50.0\ MV) \\ &= \pm 50.083\ MV \text{ or } 100\% \text{ of peak value} \end{aligned}$$

Comparator accuracy for the Tektronix S-3260 with comparator calibration and buffer amplifier technique is as folows:

$$\begin{aligned} &\pm[0.00166\ (200\ MV) + 1.67\ MV] \\ &= \pm[0.332\ MV + 1.67\ MV] \\ &= \pm 2.002\ MV \text{ or } 1\% \text{ of peak value} \end{aligned}$$

In addition to comparator resolution there is an accuracy specification of the single shot time (ΔT) measurement system on the Tektronix S-3260 of:

$$\begin{aligned} &\pm\ (1.0\% \text{ of range} + 1\% \text{ of reading} + 2ns) \\ &= \pm\ (0.01\ (100\ ns) + 0.01\ (40\ ns) + 2.0\ ns) \\ &= \pm\ (1.0\ ns + 0.4\ ns + 2.0\ ns) \\ &= \pm\ (1\% \text{ of reading} + 3\ ns) \end{aligned}$$

Worst case overall error for the rise time measurement is ± (2.25 percent (value) +3 ns) or 9.75 percent error for a 40 ns limit reading.

This accuracy can be improved somewhat by making the measurement twice and averaging the two. In using this technique the start and stop pins are reversed in the second measurement and averaged to remove the error caused by comparator skew. Tektronix claims a 50 percent increase in accuracy using the method described in Tektronix application note AX-4403 published in March 1980.

The overshoot measurement is made using the same conditions as rise time. The accuracy on this measurement is limited only by the comparator accuracy and resolution. For a maximum allowable overshoot of 50 percent using the buffer amplifier with the comparator calibration technique, the accuracy is:

$$\begin{aligned} &\pm (0.00166\ (\text{value}) + \text{resolution}) \\ &= \pm (0.00166\ (300\ \text{MV}) + 1.67\ \text{MV}) \\ &= \pm (0.498\ \text{MV} + 1.67\ \text{MV}) \\ &= \pm 2.17\ \text{MV or } 1.08\% \text{ of the } 200\ \text{MV pulse} \end{aligned}$$

Bandwidth is determined by calculation from the value obtained in the rise time measurement. This equation, as given in MIL-M-38510/101, is:

$$\text{BW (MHz)} = \frac{0.35 \times 10^3}{\text{rise time (ns)}}$$

The measurement of slew rate is made by driving the DUT input directly from the DUTIN pin (Figure 14) with a -5.0 volt to +5.0 volt step and measuring the time of the output transition time at DOUT from -2.5V to +2.5V. In this case the test-system comparator error is very small due to the large voltage swing. The error due to the single shot-time measurement system for a maximum 50 V/μs slew rate is:

$$\begin{aligned} \Delta T \text{ error} &= \pm (1\% \text{ of range} + 1\% \text{ of reading} + 2\ \text{ns}) \\ &= \pm [0.01\ (100\ \text{ns}) + 0.01\ (100\ \text{ns}) + 2\ \text{ns})] \\ &= \pm (1\ \text{ns} + 1.0\ \text{ns} + 2\ \text{ns}) \\ &= \pm 4.0\ \text{ns or } \pm 4.0\% \text{ at a } 50\ \text{V}/\mu\text{s slew rate} \end{aligned}$$

Settling time is defined as the time required for the output voltage at DOUT to settle to within ±2 percent of its final value with the input of ±5.0V as in slew rate. This measurement has the combined errors of comparator resolution, due to the very small difference in output voltage, and the error of the ΔT subsystem. A software system comparator-calibration technique was used, as in the rise time measurement, to minimize the comparator level error.

$$\begin{aligned} \text{Comparator Error} &= \pm (0.00166\ (100\ \text{mV}) + 1.67\ \text{mV}) \\ &= \pm 0.166\ \text{mV} + 1.67\ \text{mV} \\ &= \pm 1.83\ \text{mV or } \pm 1.83\% \text{ of the } 100\ \text{mV level} \end{aligned}$$

The ΔT subsystem error for settling time for a maximum 800 ns measurement is:

$$\begin{aligned} \Delta T \text{ error} &= \pm (0.01\ (1.0\ \mu\text{s}) + 0.01\ (800\ \text{ns}) + 2\ \text{ns}) \\ &= \pm (10\ \text{ns} + 8\ \text{ns} + 2\ \text{ns}) \\ &= \pm (1.0\%\ (\text{value}) + 12\ \text{ns}) \end{aligned}$$

Worst case overall error for the settling time measurement is ± (2.83 percent (value) + 12 ns) or ± 4.33 percent of the 800 ns limit. (Note: The calculation was made assuming a linear settling characteristic.)

6. REPEATABILITY

Measurement repeatability is primarily a function of the test system's accuracy and ability to provide a fast rise time, abberation free input pulse to the device under test. With the use of large general purpose automatic test equipment and the low level signals involved, noise is also a problem. Since these large test systems were primarily designed for large pinout digital testing, there are long signal lines which are subject to losses and noise pickup. This is not a problem when testing devices at TTL or CMOS logic levels but can be significant when dealing with 50 millivolt pulses. For the signal levels needed for these tests we conclude that general purpose automatic test equipment will not provide the accuracy and repeatability required. In our repeatability tests of sample devices, a repeatability error of 15 percent was achieved for rise time and overshoot measurements. A repeatability error of 2 percent was measured on the higher signal level slew rate and settling time tests.

The unacceptable level of repeatability experienced with this test equipment would be improved greatly with the use of optional test equipment such as programmable pulse generators and waveform digitizers. These options, when used with good fixturing techniques, may provide the necessary signal resolution to test low level ac parameters in an ATE environment.

SECTION V

TEST DEVELOPMENT FOR THE LM111 COMPARATOR

1. OBJECTIVE

The conventional method of testing the comparator is given in MIL-M-38510/-103 and the test circuit is shown in Figure 16. This method is identical to the one used for the LM108A operational amplifier, i.e., use of a null-feedback amplifier to keep the output within the linear range.

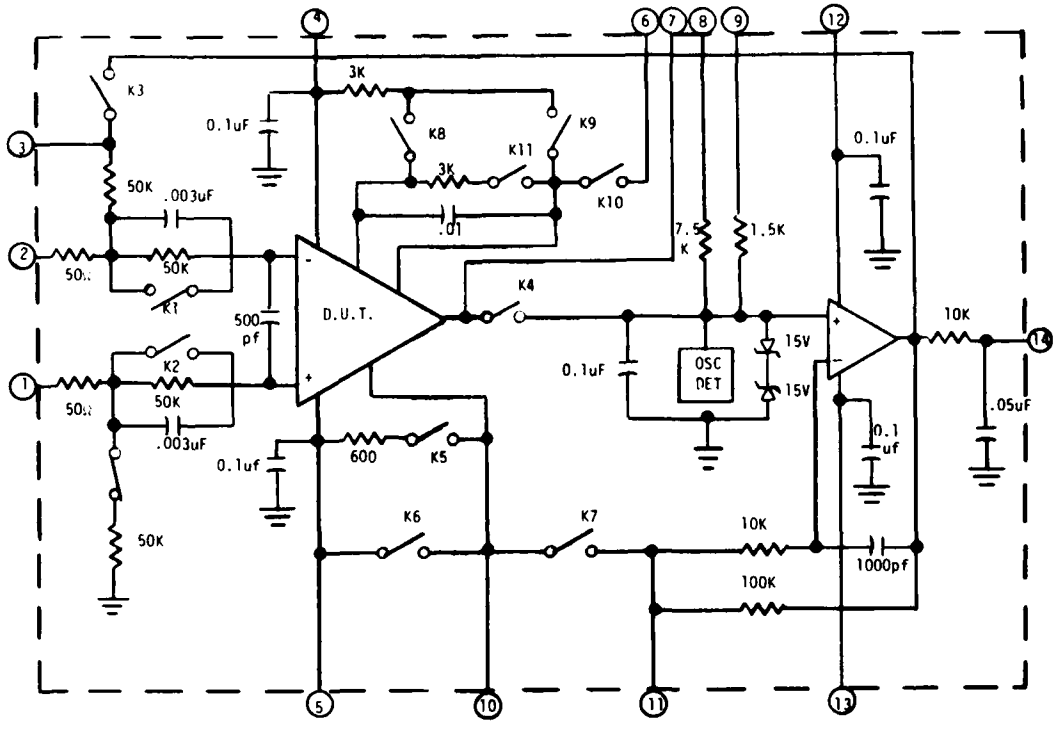

Figure 16. MIL-M-38510/103 Comparator Test Circuit

The difficulties experienced with the null-feedback method are amplified because the comparator is designed as a bistable device used as a high-speed

switch. Although the test procedures in MIL-M-38510/103 can give accurate, repeatable results, the test-circuit-fixturing layout and device compensation are very critical.

The objectives of the LM111 tests are to:

1 Develop a test method that does not need a null amp,

2 Minimize fixturing complexity,

3 Eliminate need for precision circuit elements,

4 Identify ATE-related variables.

2. SUMMARY

A new test method was developed using general purpose ATE, which tests the comparator in a manner similar to its application as a switch rather than the current method which tests the comparator as an operational amplifier. One of the advantages of this new method is that precision value components are not required and it does not have any particularly acute layout problems. A disadvantage of the new method is that test time is increased due to the iterative sequence of measurements.

A test program was written for all of the MIL-M-38510/103 static tests and the measurements data logged for successive tests using three different groups of LM111 comparators. Repeatability studies show that all of the tests except open-loop gain have a less than four-percent repeatability error. The open-loop gain measurements showed a repeatability error of up to 10 percent.

Our proposed test method gives repeatable results without the potential stability problems inherent in the null-feedback amplifier approach.

The methods developed for the LM111 comparator proved highly satisfactory. The test method, circuit (Figure 17), and procedure recommended for addition into MIL-STD-883 method 4001, Input Offset Voltage and Current and Bias Current, follows.

Procedure: Increase the value of VIN in a positive direction from a negative value until the output comparator detects a high to low transition.

Input Offset Voltage VIO

This test is performed with both switches in the closed position

$$VIO = \frac{(VIN)(R2)}{R1 + R2}$$

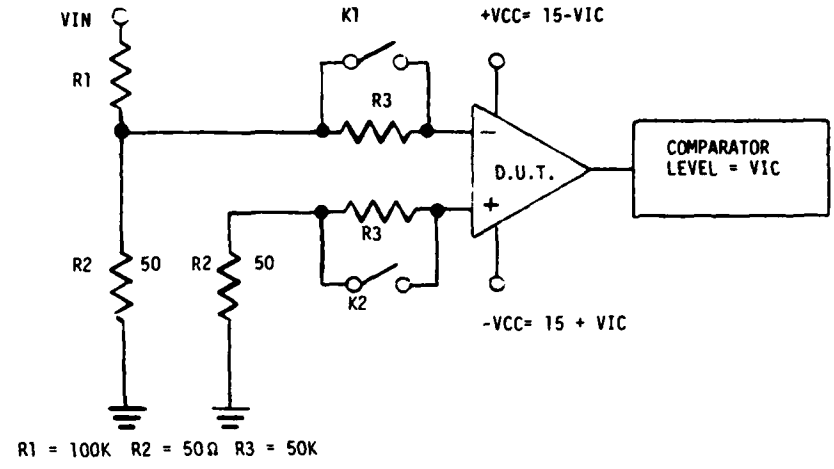

Figure 17. Proposed Test Method for MIL-STD-883 Method 4001

Positive Input Bias Current + IIB

Measure VIO (1) with Switches K1 and K2 closed.
Measure VIO (2) with Switch K2 open.

$$+IIB = \frac{VIO\ (2) - V1O\ (1)}{R3}$$

Negative Input Bias Current - IIB

Measure VIO (1) with switches K1 and K2 closed.
Measure VIO (2) with switch K1 open.

$$-IIB = \frac{VIO\ (1) - VIO\ (2)}{R3}$$

Input Offset Current IIO

Measure +IIB and -IIB
IIO = (+IIB) - (-IIB)

3. TEST DEVELOPMENT

The test circuit currently in use in MIL-M-38510/103 is shown in Figure 16. This circuit uses 38 discrete parts, an oscillation detector, and a M38510/10101 op amp to make dc tests on a comparator. A test fixture was constructed to evaluate this test circuit. Preliminary evaluation of this fixture revealed that additional decoupling of all power supplies was required to obtain repeatable results on most tests. The open-loop gain tests remained unrepeatable, prone to oscillation, and required a second fixture to be built specifically for the gain measurements.

4. CIRCUIT DESCRIPTION

The test circuit designed for this study of LM111 comparator on ATE can make all of the measurements of the previous circuit with the advantages of no null amplifiers, no precision or matched resistors, and the ability to test the comparator as a bistable device. The completed test fixture for the Tektronix S-3260 is shown in Figure 18.

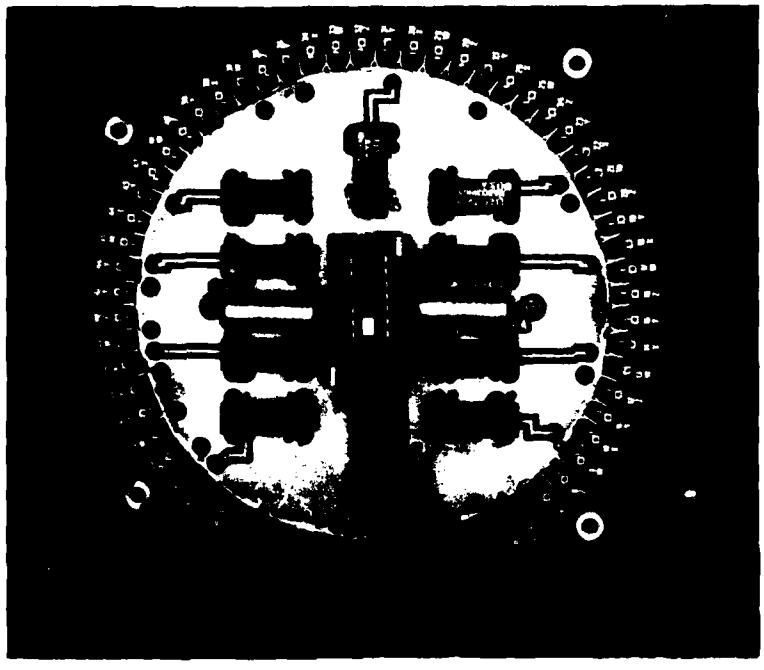

Figure 18. LM111 Automatic Test Fixture

The test circuit schematic appears in Figure 19. R1 and R2 form a voltage divider of about 2000:1 to supply the microvolt-level signals necessary for good resolution. The actual values of these resistors are not important as long as they are accurately measured (0.1%) and included in the test program. The S-3260 driver resolution is 10 mV, which when attenuated by the divider, gives 5 μV resolution. Maximum compliance is 30V/2000 = ±15 mV.

Resistors R3 and R4 form another voltage divider used for additional compliance during the input offset adjustment measurements. This divider is about 200:1, and the actual resistor values are included in the test program. The total range using this divider is about ±150 mV. Resistors R5 and R6 are inserted in series with the inputs to measure bias current. To simplfy the fixture requirements, the values of these resistors need not be matched as long as IIO is taken from the calculation [(+IIB) - (-IIB)].

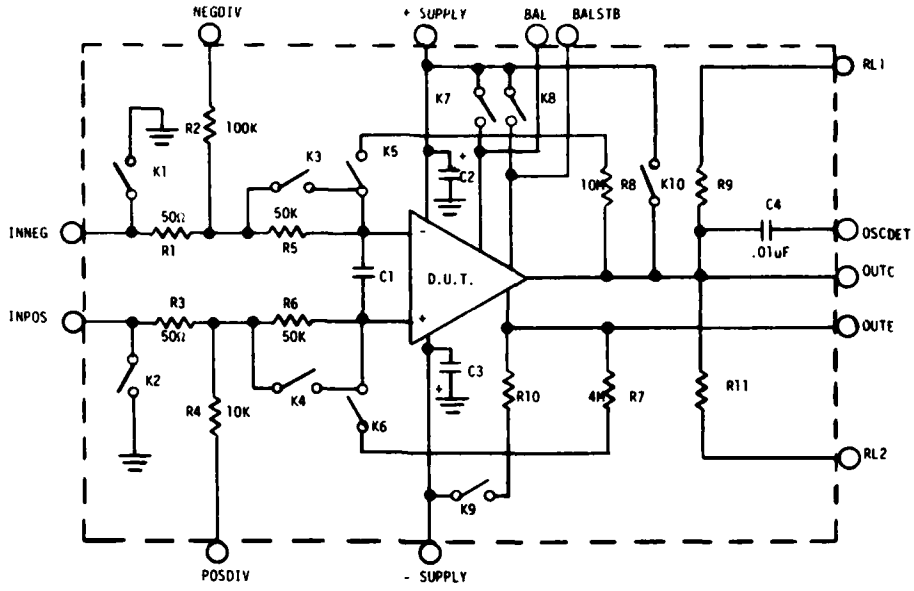

Figure 19. Automatic Test Equipment Comparator Test Circuit

Although it has been reported that a semiconductor manufacturer claims that the best way to measure input currents is to do so directly because high source resistance and stray capacitance may cause oscillation, we have not observed any oscillations using this method on any of the three groups tested.

The steps of the basic measurement loop follow:

1 Force NEGDIV with large negative voltage to latch the output high. Detect the output transition at OUTC by setting the test system comparator trip level at the midpoint of +VCC and -VCC.

2 Increment the voltage at NEGDIV in positive direction until the voltage at OUTC trips the test system comparator. To reduce measurement time and maintain precision:

a Set increment at 1V per step; continue until high-to-low transition is attained or maximum driver voltage is reached (nonfunctional).

b Set increment at 0.1V per step; continue until low-to-high transition is reached.

c Set increment at 0.01V per step; continue until high-to-low transition is reached.

d The voltage at NEGDIV is then measured with the dc subsystem in the differential mode for increased accuracy. Input-offset voltage can then be calculated from the following equation.

$$VIO = \frac{VIN\ (R1)}{(R1 + R2)}$$

Resistor matching is not necessary since the voltage developed across resistors R1 and R3 is only 100 nA x 50Ω = 5 μV at the 100 nA IIB limit. There is no need to use hard-to-obtain and costly precision resistors. The actual test circuit resistance is measured instead by a standard laboratory digital ohmmeter. Typical measurement accuracy of such a meter is better than 0.1 percent and the temperature coefficient of the resistors can be neglected if they are not exposed to the device test environment.

Worst-case accuracy is determined by the values of the resistor divider and the dc subsystem measurement accuracy. The worst-case accuracy of the measurement circuit is:

DC subsystem	±(0.1% + 10 μV)
Resistor divider	±0.2%
Divider resolution	+ 5 μV
Maximum Worst-Case	±(0.3% + 15 μV) or 0.8% of 3 mV VIO limit.

5. TEST PARAMETERS AND ACCURACY

Input offset voltage (VIO) is measured with the basic measurement sequence mentioned in subsection 4. During this test, relays K1 through K4 are closed. It is important to note that although the values of R1 and R3 are measured and used in the software test program, there is another source of error which can affect the measurement accuracy. This is the resistance to ground from INNEG and INPOS. The relays K1 and K2 should be mounted physically and electrically close to the DUT to keep this resistance to a minimum. This value of contact resistance, typically 50 mΩ to 70 mΩ was also included in our test program as part of the R1 and R3 values for increased accuracy. The open collector output is pulled up through resistor R9 by a voltage source at RL1. The emmitter is tied via pin OUTC to a voltage source at the negative supply level. The overall measurement error for VIO is the basic measurement circuit error of ± (0.3% value + 15 μv) or ± 0.8% of the 3 mV VIO limit.

Input bias current is measured by making two VIO measurements. One with K3 and K4 closed, and the other with K3 or K4 open for -IIB and +IIB respectively. Bias current can then be calculated by:

$$-IIB = \frac{\Delta VIO}{R5}$$

$$+IIB = \frac{\Delta VIO}{R6}$$

where ΔVIO is the difference between the two VIO measurements.

The expected accuracy is the same as VIO with the additional tolerance of R5 or R6. The worst case accuracy of the measurement is:

DC subsystem	$\pm$ (0.1% (value) + 100 μV
Resistor divider	0.2%
R5 or R6	0.1%
Divider Resolution	+ 5 μV
	0.4% + 105 μV

Since the voltage developed across the 50KΩ resistor at the 100 na limit is 5 mV then:

$$\text{IIB (error)} = 0.4\% + \frac{105\ \mu V\ (100)}{5\ mV}$$

$$= 0.4\% + 2.1\%$$

$$= 2.5\% \text{ of 100 na IIB limit}$$

Input offset current (IIO) is measured in MIL-M-38510 by inserting a large resistance in series with both inputs (K3 and K4 open). MIL-M-38510 requires that resistors R5 and R6 be matched to within 0.1 percent to preserve measurement accuracy. An alternate approach is to use standard unmatched resistors and calculate the value of IIO from the equation:

$$\text{IIO} = (+\text{IIB}) - (-\text{IIB})$$

Since the IIO measurement is performed by making two IIB measurements, the fixed error from the resistor divider tolerance and the error due to the dc subsystem offset drop out and the expected worst case error is approximately:

$$\text{IIO error} = \frac{\text{R5 (error) (IIB-)} + \text{R6 (error) (IIB+)}}{\text{IIO}}$$

$$= \frac{0.001\ [(\text{IIB+}) + (\text{IIB-})]}{\text{IIO}}$$

If it is assumed that IIB + $\approx$IIB- and IIB $\approx$10 IIO, then IIO error = 0.001 [10 (IIO) + 10 (IIO)]/IIO = 0.02 or 2 percent.

The difference in measured values between this technique and bench measurement is about 200 pa or about 2 percent of the 10 na limit at 25°C.

6. GAIN STUDIES

If a specific value for open-loop gain is required, then a proper methodology must be established. During our evaluation of the existing MIL-M-38510 test procedures, significant problems emerged. The measurement of open-loop gain on a comparator is difficult because the gain test requires operating the device under conditions not found in normal application.

The MIL-M-38510 test procedure is used to test collector open-loop gain while holding the output at 0.0V, +15V, and -10V with a collector pullup resistor of 1.5 KΩ connected to +30V. The output transistor emitter is connected to the negative supply terminal (-15V). Maximum heating occurs in the device chip when the output voltage is +7.5 volts. At this point, there is 15 mA of collector current and the power dissipated in the output transistor is:

PD = VCE (IC) = (15.0V + 7.5V) (15 mA) = 337.5 mw

This level of power dissipation is not one of the output levels in the specification but should be considered when manual test techniques are used. The worst case power dissipation at specified output levels is at the output voltages of 0.0V and 15.0V. During these two conditions the power dissipation is:

P_D = VCE (IC) = 15V (20 ma) = 300 mw (at VOUT = 0)

P_D = VCE (IC) = 30V (10 ma) = 300 mw at (VOUT = 15V)

At this level of power dissipation the rise in junction temperature can be calculated by:

ΔTJ = PD (θJA) where θJA = 150°C/w, as found in MIL-M-38510/103 paragraph 1.2.6
= 300 mw (150°C/w)
= 45°C

This large change in junction temperature affects the operating point of the amplifier causing a false negative gain in some cases and a definite error in the gain-measurement value. The condition can also lead to oscillation when current limit/thermal shutdown circuitry becomes active.

Another problem encountered is that the gain measurement causes the maximum power dissipation and operating temperatures to be exceeded when performing the test at 125°C. Under these conditions the total power dissipation (PDTOTAL) is:

PDTOTAL = PD (nominal) + PD (output transistor)
= 135 mw + 300 mw
= 435 mw

The maximum rated package power dissipation for the 8 lead TO-5 can per MIL-M-38510/103 is:

PD MAX (125°C) = 330 mw

Since the device is dissipating 435 mw during the test we are exceeding the maximum package limit by 105 mw, as shown below:

PD over max = 435 mw - 330 mw
= 105 mw

The junction temperature under these conditions is:

$$\begin{aligned} TJ &= 125°C + PD\ (\theta JA) \\ &= 125°C + 435\ mw\ (150°\ C/W) \\ &= 125°C + 65.25°C \\ &= 190.25°C \end{aligned}$$

This junction temperature exceeds even the maximum storage temperature by more than 40°C. Under these conditions specified for open-loop gain measurement in MIL-M-38510 device reliability, stability, and performance could be severely degraded.

Our implementation of the gain measurement uses a 6.8 KΩ resistor (R9) for the collector output pullup. Collector current is reduced with this value and power dissipation is lowered to a safe value.

During the collector gain measurement relays K1 through K4 are closed as in the VIO measurement, and relay K5 is closed to provide negative feedback to stabilize the operating conditions. With a value of 10 MΩ for R8 the maximum value of collector gain is:

$$AVC\ (Max) = \frac{R8}{R1} = \frac{10 \times 10^6}{50} = 200{,}000$$

Emitter gain is performed in a similar manner using negative feedback from the emitter to the noninverting input through R7 with relay K6 closed. In this configuration the open collector output is connected to +VCC by closing K10 and the output voltage measured at terminal OUTE. Under these conditions using a value of 4 MΩ for R7 the maximum value of emitter gain can be calculated by:

$$A_{VE}\ (MAX) = \frac{R7}{R3} = \frac{4 \times 10^6}{50} = 80{,}000$$

With the use of negative feedback and reduced collector current, circuit stability is substantially increased. Repeatability is typically better than 5 percent on all measurements.

Figure 20 displays +AVC (V/mV) versus serial number for three groups of LM111 devices. Each serial number was data logged ten consecutive times and the results showed within 95-percent repeatability for all but 4 devices from one manufacturer which exhibited oscillation problems verified in bench testing. Serial numbers 44 through 47 exhibited oscillation.

7. REPEATABILITY

The shmoo plots in Figures 21 through 23 show the results of repeatability analysis on three groups of LM111 comparators from different manufacturers. Figure 21 shows the measured value of input offset voltage

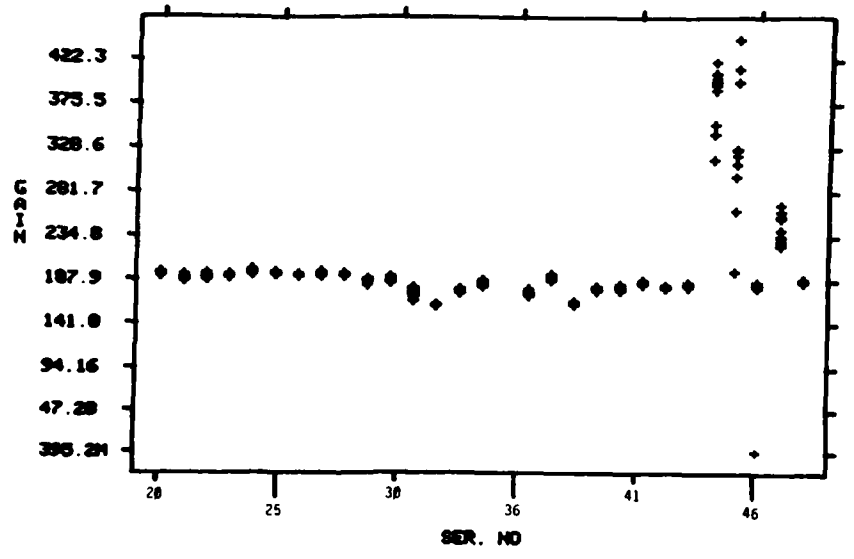

Figure 20. Repeatability Gain versus Serial Number for the LM111 at T_A = 25°C

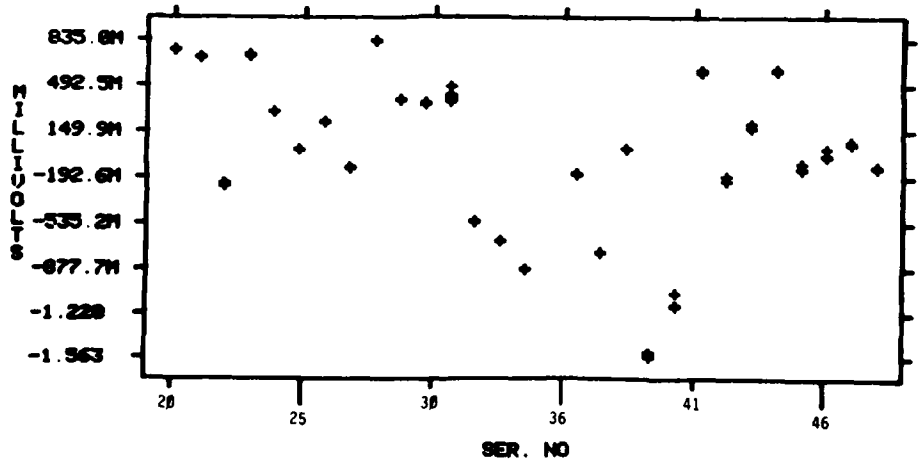

Figure 21. VIO Value versus Serial Number at VCM = 0.0V, T_A = 25°C (10 Consectutive Measurements)

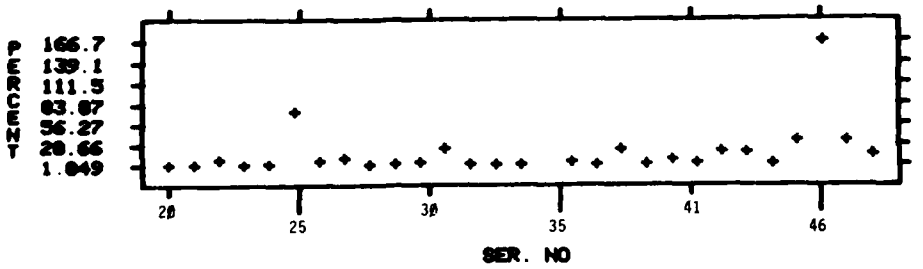

Figure 22. Worst-Case Repeatability Error versus Serial Number at VCM = 0.0V, T_A = 25°C

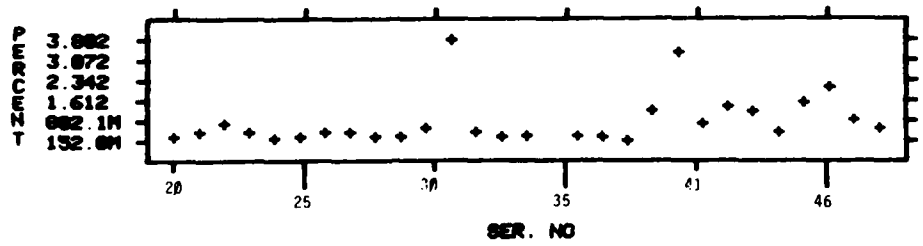

Figure 23. Normalized Repeatability Error versus Serial Number at VCM = 0.0V, T_A = 25°C

logged 10 consecutive times for each device serial number. Figure 22 is a plot of the calculated worst case repeatability from the equation:

$$\% \text{ repeatability error} = \frac{[\text{VIO (max)} - \text{VIO (min)}](100)\%}{\text{VIO (min)}}$$

It can be seen from this plot that as VIO (min) gets closer to zero the percent of error can get very large even when the error is extremely small (+5 μV). To minimize this effect, each value of repeatability was normalized to the measurement limit. This was accomplished by the following formula:

$$\% \text{ Normalized repeatability error} = \frac{[\text{VIO(max)} - \text{VIO (min)}](100\%)}{\text{VIO (limit)}}$$

is which the normalized repeatability error is shown in Figure 23.

This normalization of the error calculation shows the true repeatability of the test system. From a sample size of 280 measurements the lowest value was 0.152 percent and the highest 3.8 percent with a mean repeatability error of 0.85 percent for the VIO measurement. For a test limit of 3 mV for the VIO measurement the mean value is 0.0085 (3 mV) = 25.5 μV or ±12.75 μV.

All measurements using the ATE alternate method showed a worst case repeatability error of less than 4 percent except gain (Table 3).

The direction of the increments in the ATE measurement loop will not affect the resolution or accuracy of the test method due to hysterisis. If the direction is changed on the input increment, then the output transition direction will also change.

TABLE 3. NORMALIZED REPEATABILITY ERROR FOR LM111 TESTS

Test	Parameter	Max Percent Error	Mean Percent Error	Test	Parameter	Max Percent Error	Mean Percent Error
1	VIO	0.3	0.12	19	+VIO(ADJ)	1.95	1.08
2	VIO	0.6	0.48	20	-VIO(ADJ)	1.02	0.72
3	VIO	0.15	0.11	21	CMR	1.37	0.82
4	VIO	0.3	0.15	22	VOL	0.25	0.10
5	VIO(R)	0.15	0.069	23	VOL	0.12	0.11
6	VIO(R)	0.30	0.193	24	VOL	0.06	0.04
7	VIO(R)	0.15	0.096	25	VOL	0.06	0.03
8	IIO	0.95	0.95	26	ICEX	2.0	1.38
9	IIO	3.81	2.77	27	II1	0.9	0.55
10	IIO	0.95	0.95	28	II2	0.6	0.50
11	IIO(R)	0.76	0.34	29	+ICC	2.5	1.89
12	+IIB	0.19	0.14	30	-ICC	3.3	2.19
13	+IIB	0.66	0.42	31	IOS	3.6	2.56
14	+IIB	0.29	0.15	93	+AVC	2.67	1.94
15	-IIB	0.19	0.095	94	-AVC	8.29	6.34
16	-IIB	0.52	0.351	97	+AVE	8.99	5.21
17	-IIB	0.19	0.060	98	-AVE	4.26	3.28
18	VO(STB)	0.35	0.032				

Note: $T_A = 25°C$

SECTION VI

INDUSTRY SURVEY

A survey of several industry users and suppliers of linear microcircuits was performed for general comments on the value of MIL-M-38510 and MIL-STD-883 test conditions and procedures. It was stated to each of the industry contacts that the objective of the RADC task is to simplify the testing of op amps and comparators using automatic test equipment and to define ATE-related variables. Comments on the military specifications from applications or reliability viewpoints were solicited. Identification of measurements that are required by MIL-M-38510 and that are not amenable to automatic test procedures because of difficulty or nonrepeatability were asked for.

The solicited contacts all reported difficulties with the dynamic tests, true rms value requirements, noise measurements, and ac measurements. Most used bench tests when trying to comply with MIL-STD-883.

Most of the 12 users and the 12 suppliers contacted felt that a precise open-loop gain measurement value was not that important. The design engineer seldom needs an absolute value; a guaranteed minimum is usually sufficient. Most only attempt open-loop gain measurement as a bench-type test, have reasonable success, and find the results fairly repeatable. None of those contacted claim high levels of success with automatic test equipment. Most also found the open-loop gain test to be tedious and time consuming.

Discounting the obvious problems with open-loop-gain testing and gain tests on comparators, the major technical problems encountered with the MIL-M-38510 slash sheets have been resolved without extreme difficulties. Complaints were made on the many changes to MIL-M-38510 and their inability to adequately keep abreast of the changes. Just to correct obvious errors, typographical or other, was difficult. No specific MIL-M-38510 problems were flagged. Most contacts expressed a willingness and necessity for compliance with existing documents and accepted the system the way it is.

Users and suppliers offered no tangible suggestions for more appropriate linear-circuit testing. Comments ranged from suggestions for characterization of the devices in the laboratory to complete rewriting of the specifications to meet their needs.

Most users/suppliers reported little to no experience with chip heating or related problems. Some contacts stated that the usual MIL-M-38510 slash sheet sequence of tests with the higher current tests last were satisfactory, but wait statements were sometimes used, if stability and repeatability appeared to be

affected by thermal equilibrium. In most cases it was found they rearranged the test sequence to fit their own requirements.

Overshoot and slew-rate testing is conducted almost exclusively on the bench. Few contacts have attempted these tests with automatic test equipment.

In general the comments indicated stability of devices during test is under control because most tests were performed per MIL-STD-883 on the bench. Some special interface units have been devised. Certain op amps have been more susceptible to problems than others.

Some of those contacted had problems with noise and oscillations when using ATE. This was not a problem with MIL-STD-883 test methods or with MIL-M-38510 slash sheets, but rather with implementation of the tests using automatic test equipment. The general consensus was that the use of decoupling capacitors and ferrite beads minimize most problems of this nature and that the use of these devices must continue to be allowed.

With respect to the success the users and suppliers have had with performance of ac and dc tests in the same fixtures, there has been no real progress. Some minimal success at the lower frequencies or rise times has been reported. Many testers in use are lower-level digital types and do not do switching times. Most of those contacted switch back and forth between ac and dc test fixtures depending on machine types and levels of sophistication of test equipment.

SECTION VII

CONCLUSIONS AND RECOMMENDATIONS

Testing of linear high performance amplifiers and comparator microcircuits can be performed reliably on general purpose automatic test equipment with only minor changes to existing test requirements. This device testing can be simplified by deletion of the null amp and taking maximum advantage of measurement systems and computational ability of automatic test equipment. This removes the need for expensive precision fixture components and the time and talent necessary for complex fixture construction.

A recommended change to MIL-M-38510/101 and MIL-M-38510/119 is inclusion of the circuit of Figure 4, found in Section III, as either a primary or alternate test circuit for Group 4, subgroup 1 through 6 testing (static and dynamic tests). The stability of the circuit has proven to be superior to the existing circuit for use on the automatic test equipment.

The increased stability resulted from a reduction in circuit components from more than 30 parts to 22, which minimized layout problems while still complying with MIL-STD-883 test methods. Results of the repeatability studies for the TL061 and LM108A operational amplifiers indicate that accurate and repeatable data can be obtained using the new circuit. IIO measurements proved to be an exception. One answer for this problem would be to actually measure IIO instead of calculating it from IIB measurements. Implementation of this solution would be simple. The only change required would be opening both K2 and K4. Take measurements at EOUT and derive IIO from the following equation:

IIO = ((E1-E2)/Loop Gain)/((R4+R5)/2) where E1 is defined as EOUT with both K2 and K4 closed. E2 is EOUT with both K2 and K4 open.

The minimum limit approach for testing minimum open-loop gain would also be a recommendation for inclusion into MIL-M-38510 since absolute gain value is reportedly being proposed for deletion by the industry.

Transient response and noise tests require signal levels and test sensitivities beyond that found on general purpose ATE. These tests, evaluated on the TL061 and LM118, proved to be inaccurate and unrepeatable with the available equipment. It is felt however that a suitable test can be performed on ATE given more elaborate fixturing using buffer amplifiers, waveform generators, and signal digitizers. This could be a subject for further study.

The methods developed for the LM111 comparator proved highly satisfactory. The test method, circuit (Figure 17), a procedure is recommended for addition

into MIL-STD-883 method 4001, Input Offset Voltage and Current and Bias Current and is described in section V-2. The only disadvantage of this method is that it uses an iterative measurement technique which can give a worst case test time of 1 second per measurement. This increased test time can be reduced, however, by starting at a worst case input value which gives a pass-fail indication only.

It is also recomended that the comparator test procedures in MIL-M-38510/103 be changed to limit the power dissipation to a much lower value (less than 300 mw) during gain measurements. This change will prevent overstress of the device and can improve measurement accuracy and repeatability.


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